SNS Timing System Preliminary Design Review

April 20, 2000

Review Committee:

Marc Ross (SLAC) Chair
Lawrence Donley (ANL)
Ken Reece (ORNL)

Charge to Committee:

- Is the scope well defined?
- Are the system functional requirements well defined and documented?
- Will the design as presented meet those requirements?
- Are the interfaces and work allocations well defined?
- Are there missing or ill-conceived elements?
- Is the implementation plan reasonable?
- Are the schedule and cost estimate credible?
- Any issues or advice?
- Are we ready to proceed with the final design?

The SNS timing system is designed to provide pulse triggers to a variety of users. The triggers must be synchronized with the beam to within 2 ns. The timing system must also synchronize the beam pulses with the neutron velocity choppers and the electrical powerline from TVA.

The committee was presented with an overview (D. Gurd) which contained the charge listed above, a design for timing and event distribution (B. Oerter), a scheme for locking the system to the powerline (R. Nelson), and an outline of the chopper system (D. Abernathy). We were also presented with a resource and schedule overview (B. Oerter and W. DeVan).

The three technical presentations covered the system well. The designs presented will meet the specified requirements.

As presented, there were a few missing items, but each of the key pieces (synchronization, event generation, encoding/decoding, distribution and trigger generation) appears well designed and properly functional. We identified missing interface hardware, especially between the beam permit system and the chopper controllers and between the chopper controllers and the ring extraction kicker trigger. Also, the provision should be made to allow the diagnosis of event strings. This is needed at only one location, presumably next to the encoder. The project staff had also recognized the need for these additions.

Our most serious recommendation falls under the heading of functional requirement definition. The committee unanimously concluded that the requirements for line synchronization require further evaluation. The quality of the line lock, the expected rate of phase variation, the quality of the chopper synchronization and the allowed phase error of the linac pulse timing with respect to the powerline are critical to the expected performance of SNS and are incompletely understood and specified. The piece of the timing system most affected by the lack of definition is the LANL reference timing controller.

Without a detailed understanding of the line lock constraints, a proper SNS-wide system optimization cannot be done. A serious concern was the expected veto rate as a function of extraction gate width. We understood that that indicated a significant reduction in the useful beam for experimenters as a function of the quality of the powerline phase stability. The project should try to reduce the veto rate as much as possible and the committee had several suggestions that seem reasonable but do not pertain directly to the timing system.

We recommend that the project evaluate the linac sensitivity to incoming line phase transients or, more simply, as a function of phase error between the powerline and the linac pulse time. There now exist several examples of RF systems with minimal sensitivity to powerline phase. Some members of the committee felt that the performance of existing linacs (SLAC, CEBAF) was sufficiently good in this regard to encourage serious investigation of linac linelock tolerances. The most commonly blamed source of linac-lock sensitivity is 'heater-hum' caused by the raw 60 Hz AC used for the klystron filament. Several techniques have been used to counter the problem: 1) DC filament power and 2) suppression of the filament voltage during the pulse using a chopper. Either of these, if the cost is reasonable, would allow a considerable tightening of the line lock 60 Hz phase locked loop. The chopper control would be simpler, and the pulse to pulse timing errors that contribute to a substantial fraction of the gate error would be reduced. The project should use the test system at LANL to determine if this is the biggest source of line-lock sensitivity.

We questioned the projected performance of the accumulation ring in connection with the veto rate. If the ring can retain the beam for more than just a few turns, then the timing requirements are not quite as tight and the chopper derived extraction trigger window could be increased. It is not clear how the ring can accumulate beam for 1000 consecutive turns and retain it for only a few (10 or less). For this to be true, the instability threshold must be known to a few percent, which is unlikely. We were concerned that the threshold for instability would be lower, thereby reducing the accumulation time and effectively reducing the beam intensity on target.

Beyond the above, the committee felt that a better understanding of the powerline transients, or equivalently, a detailed specification of the 60 Hz PLL performance would allow a significant increase in the effective gate width. If a determination of the error in the 600 Hz pre-trigger could be made and corrected with a simple feedback system the gate error would also be reduced. While such a feedback system would be an extension of the system beyond what was presented, we felt it is required in order to reduce the +/- 5 us error ascribed to 'fast' variations of the powerline phase. Such variations, if they exist, will cause instantaneous changes in the chopper rotation and therefore can be smoothed by tightening of the bandwidth of the 60Hz PLL. Of course, the sensitivity of the linac to the phase errors must be specified in concert.

It would be useful, for other projects as well, to categorize the sources of pulse timing error: determining both their magnitude and character. Are they random or systematic?

There were a number of additional, less serious concerns.
1) How is the required number of modes determined? We felt that the functional requirement for the number of modes needed for various types of operation should be specified. In addition, some users will develop hardware that uses hard-decoded modes. Since the number of modes is limited, the rules for their use should be published so that their availability is maximized.
2) We saw some attempt at redundancy, but were not presented with an overall system redundancy plan.
3) We had one concern regarding the schedule. There should be a milestone on the schedule for the delivery of a model timing system to be used for front end testing at LBL.
4) Along the same line, it was clear from the project budget that no resources had been allocated for the distribution of model timing systems to the collaborating labs; to be used for hardware testing and system development.
5) Project staff noted a shortcoming in FTE resources allocated to the project.