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Title: RF BOARD (155Y503003B) OF THE FRCM OVERVIEW

Author(s): T.S. Rohlev

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1 RF Description

Introduction

The radio-frequency (RF) board of the Frequency/Resonance Control Module (FRCM) measures the in-phase (I) and quadrature (Q) components of four separate RF signals and modulates and upconverts a single channel of I and Q data to an RF signal; therefore, it has four input channels and one output channel.

The four input channels have RF as an input and digital data (in the form of I,Q,-I,-Q,I,Q, etc.) as an output. The output channel has digital data as an input (in the form of an IQ pair) and RF as the output. The output channel can be connected to the input channels, allowing the board to drive itself. This is done for self-test and self-calibration.

There is a Direct Digital Synthesizer (DDS) chip on board that can provide a substitute intermediate frequency (IF) for the IQ modulator. This is done so that, if desired, the output frequency can be swept over a fairly narrow range (± 1 MHz) to track or find the cavity resonance.

This is a relatively straightforward board. The most advanced chip on the board is the DDS because it needs to be programmed. This write-up provides some guidelines for programming the DDS, but in general you should find the data sheets that came with the DDS adequate for programming.

After the DDS chip, the analog-to-digital converters (ADCs) are next in complexity, then there are the two high-speed DACs, or digital-to analog converters (one for I, one for Q). To operate the ADCs and the DACs, simply power them on. Section 2 covers the particulars of the ADCs and DACs. The rest of the board is either RF or analog.

The remainder of this section will be devoted to a detailed description of each input channel, the output channel, the self-test feature, and DDS operation.

Input Channels

The input channels are digital IQ detectors; i.e., they digitally sample an RF signal to gain information about its I and Q components. This is done by sampling the RF sine wave in effect every 90° . I and Q are a Cartesian representation of the RF vector that is normally represented as amplitude and phase. The data produced is the sequence of I, then Q, then -I, then -Q, then I, and so on. Normally the -I data is subtracted from the I data and divided by two to get the final I signal, and the -Q data is subtracted from the Q data and divided by two to get the final Q signal. This eliminates any DC offset in the measurement. To calculate the amplitude of the sine wave, use the standard formula: $A = \text{SQRT}(I^2 + Q^2)$; to calculate the phase, use the formula $\phi = \text{ARCTAN}(Q/I)$.



The RF frequency of the input channels is 402.5 MHz (with the exception of the cavity channel, which is downconverted in the tunnel and comes in at 50 MHz). Before sampling, the RF signal is downconverted to 50 MHz and filtered. The ADCs have a sampling frequency of 40 MHz, which corresponds to 450° of the input sine wave; thus the signal is still sampled every 90°, but with a whole cycle in between. See Section 3 for more information on how I/Q demodulation works.

The next four subsections describe the functions of each input channel. Because the input channels are nearly identical, the forward channel is given a complete description while the descriptions for the other channels cover only the features that differ from the forward channel.

The Forward Channel and Output Channel subsections also include test procedures.

Forward (F) Input Channel

The 402.5-MHz forward signal comes into the PKZ connector J8 and goes to an RF single-pole, double-throw (SPDT) switch (U40). The switch logic is such that a logic (CMOS) 1 selects the input signal, and a logic 0 selects the test signal. After exiting the switch, the signal is sampled by a 20-dB directional coupler (U27). The coupled signal is rectified through a diode pair (U15), low-pass filtered, and amplified with an operational amplifier (U21). The amplified quasi-DC signal is sent to the multiplexer line on J3. The passed signal then goes to the RF port of mixer U35. The local oscillator (LO) port of the mixer should be a 352.5-MHz sine wave with a 17-dBm (2.24 Vpk) level.

The LO signal distribution starts at J6, then goes to U29 where it is split 4 ways. It then goes out to each channel for amplification and connection to the LO port of the mixer. A 13-dBm (1.41 Vpk) signal should be sufficient at the LO drive at J6. The LO amplifier for the forward channel is U80. After being downconverted by the mixer, the signal goes through a bandpass filter (U4), which selects only the lower sideband (50 MHz). After leaving the filter, the signal goes through a 16:1 (ohms ratio) RF transformer that splits and amplifies the signal into two complementary pairs.

The AC voltage at the output of either leg of the transformer should never exceed 0.56 Vpk. The DC voltage at the transformer output is set by each ADC, and can vary, but should be about 2.4 V. The operation of the ADC is detailed in Section 2. The output is 14 bits, two's complement, along with an overvoltage bit (OVR) and a data-ready bit (DRY). The DRY bit is essentially the clock. The complementary encodes for the ADCs come from an emitted-coupler logic (ECL)-distribution network on the back of the board.

Forward Channel Test Procedure

To test the operation of this channel, place a 402.5-MHz signal at the input into roughly +10 dBm. Change the clock frequency from 40 MHz to 50 MHz. This allows the ADC to have a stable output because you will now be sampling a 50-MHz signal with a 50-MHz



clock. Adjust the phase of the 402.5-MHz signal until the largest possible reading is coming out of the ADC, then increase the power level until the OVR bit goes to one, as measured on the logic analyzer. This is the maximum power-out input. The output of the DAC should be very near 8192 counts. Lower the power of the 402.5-MHz signal until the noise floor of the ADC is reached. The difference between the two powers is the dynamic range, which should be on the order of 70 dB. The low-order bits with no input should all read zero, but they might look as if they don't. It is confusing to look at the bits when there is no input because once their digital equivalent is calculated, their readings are zero or near-zero.

Reflected (R) Input Channel

This is the same as the Forward channel, except that the U numbers are different.

Beam (B) Input Channel

This channel differs only slightly from the two described above in that it has a pre-amplifier added to the input because we didn't know the exact value of the beam signal available. The input on J9 first goes through a pad (U71) and is then amplified by U9 before going to the RF SPDT switch (U41). The gain of the amplifier at 400 MHz is about 13.5 dB. Currently there is a 15-dB pad in front of the amplifier, so there is a little less than zero net gain.

Cavity (C) Input Channel

The cavity differs from the other channels in that the downconversion to 50 MHz has already been performed before the signal reaches the board. The signal comes into J11 and goes to the RF SPDT switch. It exits the switch, goes to a 20-dB directional coupler (U28) and a variable pad (U73). The signal then goes into the 50-MHz bandpass filter (U8). The operation is the same as for the other channels from that point on. The peak input power on this channel is on the order of +3 dB. The test signal, which is at 402.5 MHz, must be downconverted to simulate the 50-MHz IF coming into the board. For this reason, the mixer (U37) and its accompanying LO amplifier (U79) are on the test side of the SPDT switch.

Test Signal Distribution

The RF board has a unique feature that allows the output signal to be routed to any or all of the input channels simultaneously. For this to occur, the output switch (U42) and any or all of the input switches must be in their test position. The output is first attenuated (U76) and then amplified (U10) before going to a 1:4 RF splitter (U30) for distribution to all of the channels. The pad should be chosen so that the power level of the test signal at peak output is less than what is necessary to saturate any of the channels (OVR = 1).



Output Channel

The output channel starts at the I and Q DACs (U1 and U2). These are 16-bit high-speed DACs whose operation is described in Section 2. The output of each DAC is a pair of complementary current sources that are modified to complementary-level shifted voltages by the resistor network following the DACs. The center voltage is 1.5 V, the limits are 1.2 V and 1.8 V (± 0.3 V). These voltages drive either the I and I* or Q and Q* inputs of the IQ Modulator/Mixer chip (U3).

Multiplexer lines 7 and 8 provide a converted value for the I and Q drive signals. Their range is ± 1 V, which indicates both the polarity and magnitude of the drive signal. U3 takes in the quasi-DC I and Q values and modulates them up to an IF frequency (50 MHz). The signals are then transferred to another part of the chip where they are upconverted using an LO frequency (352.5 MHz) to the final RF frequency of 402.5 MHz. The chip has a fast sleep-enable function that turns the RF drive off at the output port of the board within 320 ns of the fast-protect signal. Most of this delay is caused by the 402.5-MHz bandpass filter (U7), which follows U3.

Following the filter, there are two stages of amplification with U12 and U11. The pads in front of these amplifiers are used to prevent saturation and improve match. The output is sampled with a 20-dB directional coupler (U24), measured in the standard way (U18) and sent to the output SPDT RF switch, which either routes the signal off the board to drive the klystron or keeps it on-board for the test signals described above.

The last and most unique part of the output channel is its ability to switch out the IF frequency with another frequency generated on-board with the DDS. This allows the output frequency to be modulated without the need to rotate the I and Q vectors (which could activate inherent sideband problems). The DDS chip (U34) puts out a pair of complementary currents that go through an RF transformer and are turned into a zero-offset RF voltage. The signal is then filtered and sent to the RF SPDT switch (U44), which selects between the IF input and the DDS input. Refer to the DDS manual for information on programming the DDS chip (we use parallel inputs, not serial ones). The DDS chip also has an independent DAC output that is used as an analog voltage-out for the water system. Its range is ± 2.4 V, and it is programmable in the same sequence as the frequency source.

Output Channel Test Procedure

To test the output channel, set the bits of the I DAC to provide the maximum output and set the Q DAC to zero. Verify that the I and I* voltages are 1.8 V and 1.3 V, respectively, and that both Q outputs are at 1.5 V. Provide a 50-MHz IF drive at -10 dBm. Check that the switches are set to accept IF and to put power at the output port, and make sure that the fast-protect level is low (RF on). Put a spectrum analyzer on the output and you should see some structure at 402.5 MHz. If you adjust the I and Q levels, the strength of the signal should increase or decrease. Adjust the output pads so that the I max. or Q max. levels are about +10 dBm (radius of circle), at which point the I max. and Q max. level should be



+13 dBm (corner of the box). Toggle the fast-protect or the output switch and the signal should go away. For maximum isolation, move both of the switches to the off state.

Load a program into the DDS (after putting the master reset–MR– signal high for 10 cycles) and move the RF switch to the DDS position. The output frequency should have changed by whatever frequency you programmed around 50 MHz. If the chip is working properly, it will be hot to the touch.

This is all that is required to operate and test the RF board as a standalone unit.



2 Operation Instructions for the AD768 and AD6644

AD768 DAC

The AD768 is a high-speed 16-bit DAC. There are two of these chips on the board. Table 2-1 describes the pinouts for each chip.

Table 2-1. AD768 DAC Chip Pinouts

AD768 DAC			I DAC U1		Q DAC U2	
PIN #	Name	Value	Connector #	Connector Pin	Connector #	Connector Pin
1	IOUTA	1.2 TO 1.8 V				
2	NR	?				
3	REFOUT	2.5 V				
4	NC	NC				
5	REFCOM	GND analog				
6	IREFIN	0 V?				
7	DB0 LSB	TTL DATA	J5	55	J5	73
8	DB1	TTL DATA	J5	56	J5	74
9	DB2	TTL DATA	J5	53	J5	71
10	DB3	TTL DATA	J5	54	J5	72
11	DB4	TTL DATA	J5	51	J5	69
12	DB5	TTL DATA	J5	52	J5	70
13	DB6	TTL DATA	J5	49	J5	67
14	DB7	TTL DATA	J5	50	J5	68
15	DCOM	GND digital				
16	CLOCK	20 MHz TTL	J5	36	J5	37
17	DB8	TTL DATA	J5	42	J5	60
18	DB9	TTL DATA	J5	41	J5	59
19	DB10	TTL DATA	J5	44	J5	62
20	DB11	TTL DATA	J5	43	J5	61
21	DB12	TTL DATA	J5	46	J5	64
22	DB13	TTL DATA	J5	45	J5	63
23	DB14	TTL DATA	J5	48	J5	66
24	DB15 MSB	TTL DATA	J5	47	J5	65
25	VDD	+5V analog				
26	VEE	-5V analog				
27	IOUTB	1.8 TO 1.2 V				
28	LADCOM	GND analog				



Digital Inputs

The digital inputs use TTL values.

The DAC coding is straight binary, not two's complement.

Table 2-2 describes the coding and current/voltage outputs for the two DACs.

Table 2-2. AD768 I DAC and Q DAC Outputs

I DAC					
Digital code	level	IoutA (ma)	IoutB (ma)	I (V)	I* (V)
0	min.	0	20	1.2	1.8
32767	mid. -	10 -	10 +	1.5 -	1.5 +
32768	mid. +	10 +	10 -	1.5 +	1.5 -
65535	max.	20	0	1.8	1.2
QDAC					
Digital code	level	IoutA (ma)	IoutB (ma)	Q (V)	Q* (V)
0	min.	0	20	1.2	1.8
32767	mid. -	10 -	10 +	1.5 -	1.5 +
32768	mid. +	10 +	10 -	1.5 +	1.5 -
65535	max.	20	0	1.8	1.2

Timing

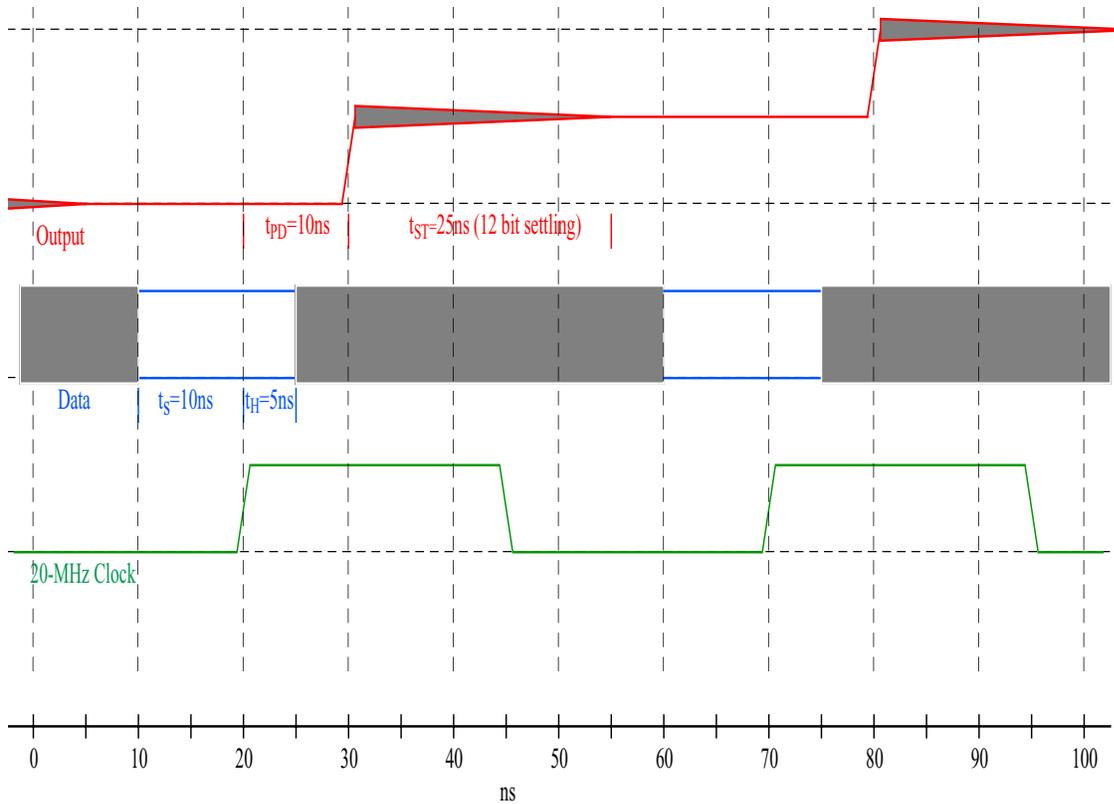
The digital timing requirements are as follows:

- Data is locked on the rising edge of the clock.
- Data must be stable for at least 10 ns before the rising edge of the clock ($t_S = 10$ ns).
- Data must be stable for at least 5 ns after the rising edge of the clock ($t_H = 5$ ns).
- The output value will begin to change 10 ns after the rising edge of the clock ($t_{PD} = 10$ ns).
- The output value will come to within 0.025% (12 bits set) of its final value 35 ns after the rising edge of the clock ($t_{ST} = 25$ ns, $t_{ST} + t_{PD} = 35$ ns).



Figure 2-1 indicates the timing of the various signals involved in the digital-to-analog conversion.

Figure 2-1. AD768 DAC Timing





AD6644 ADC

The AD6644 is a 14-bit ADC capable of running at 65 MSPS. It will be clocked at 40 MSPS and used to do the I/Q demodulation of the 50-MHz input signals from the cavity, forward, reflected, and beam data. There are four of these chips on the board; Table 2-3 describes their pinouts, and values.

Table 2-3. AD6644 ADC Chip Pinouts and Values

			BEAM		REFLECTED		FORWARD		CAVITY	
AD6644 ADC			U53		U65		U64		U66	
PIN #	NAME	VALUE	Conn.	Pin#	Conn.	Pin#	Conn.	Pin#	Conn.	Pin#
1	DVcc	3.3 V digital								
2	GND	Ground								
3	Vref	2.4V								
4	GND	Ground								
5	ENCODE	+clock 40-MHz ECL								
6	ENCODE*	-clock 40-MHz ECL								
7	GND	Ground								
8	AVcc	5 V analog								
9	AVcc	5 V analog								
10	GND	Ground								
11	AIN	+Input 50 MHz 0.56 Vpk								
12	AIN*	-Input 50 MHz 0.56 Vpk								
13	GND	Ground								
14	AVcc	5 V analog								
15	GND	Ground								
16	AVcc	5 V analog								
17	GND	Ground								
18	AVcc	5 V analog								
19	GND	Ground								
20	C1	internal Vref								
21	GND	Ground								
22	AVcc	5 V analog								
23	GND	Ground								



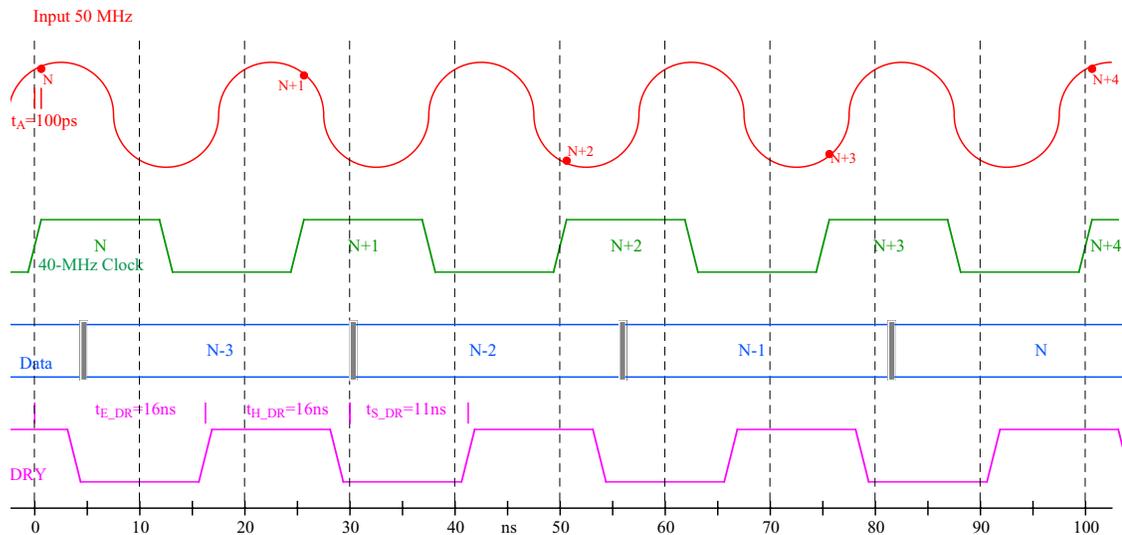
Table 2-3. AD6644 ADC Chip Pinouts and Values

AD6644 ADC			BEAM		REFLECTED		FORWARD		CAVITY	
AD6644 ADC			U53		U65		U64		U66	
PIN #	NAME	VALUE	Conn.	Pin#	Conn.	Pin#	Conn.	Pin#	Conn.	Pin#
24	C2	internal Vref								
25	GND	Ground								
26	AVcc	5 V analog								
27	GND	Ground								
28	AVcc	5 V analog								
29	GND	Ground								
30	AVcc	5 V analog								
31	DNC	no connect								
32	OVR	CMOS overrange, 1=ovr	J4	38	J4	58	J4	78	J4	18
33	DVcc	3.3 V digital								
34	GND	Ground								
35	DMID	Data midpoint DVcc/2								
36	D0 (LSB)	CMOS data	J4	37	J4	57	J4	77	J4	17
37	D1	CMOS data	J4	36	J4	56	J4	76	J4	16
38	D2	CMOS data	J4	35	J4	55	J4	75	J4	15
39	D3	CMOS data	J4	34	J4	54	J4	74	J4	14
40	D4	CMOS data	J4	33	J4	53	J4	73	J4	13
41	D5	CMOS data	J4	32	J4	52	J4	72	J4	12
42	GND	Ground								
43	DVcc	3.3 V digital								
44	D6	CMOS data	J4	31	J4	51	J4	71	J4	11
45	D7	CMOS data	J4	30	J4	50	J4	70	J4	10
46	D8	CMOS data	J4	29	J4	49	J4	69	J4	9
47	D9	CMOS data	J4	28	J4	48	J4	68	J4	8
48	D10	CMOS data	J4	27	J4	47	J4	67	J4	7
49	D11	CMOS data	J4	26	J4	46	J4	66	J4	6
50	D12	CMOS data	J4	25	J4	45	J4	65	J4	5
51	D13 (MSB)	CMOS data	J4	24	J4	44	J4	64	J4	4
52	DRY	CMOS data ready, 1=ready	J4	23	J4	43	J4	63	J4	3

Timing

The timing of the AD6644 (at 40 MHz) is described in Figure 2-2.

Figure 2-2. AD6644 ADC Timing



There is a 4-clock cycle delay between the time a signal is measured and the time the data appears at the outputs. This is 100 ns for a 40-MHz encode clock. The Data Ready signal (DRY) is active high and is an inverted and delayed version of the Encode (ENC) clock signal. The timing specifications are as follows:

- $t_A = 100 \text{ ps}$ The time between the rising edge of the ENC signal and the time the data is actually sampled.
- $t_{E_DR} = 16 \text{ ns}$ The time between the rising edge of the ENC signal and the time the data is ready (DRY high).
- $t_{H_DR} = 16 \text{ ns}$ The hold time for which there is good data after the rising edge of the DRY signal.
- $t_{S_DR} = 11 \text{ ns}$ The setup time between the data becoming stable and the DRY signal going high.
- $t_j = 200 \text{ fs}$ The aperture jitter on the device (= $3.6E-3$ degrees @ 50 MHz).



Inputs

There are two complementary analog inputs (A_{in} and A_{in}^*), each of which should be limited to 0.56 Vpk (1.1 Vpk-pk). The two signals are subtracted internally to produce a signal that is 1.1 Vpk (2.2 Vpk-pk). In the ideal case, $A_{IN} = A\sin(\omega t)$ and $A_{IN}^* = -A\sin(\omega t)$. The resultant is $A_{IN} - A_{IN}^* = 2A\sin(\omega t)$. In a more realistic case, there will be amplitude and phase differences between the signals. In such a case, $A_{IN} = A\sin(\omega t)$ and $A_{IN}^* = -B\sin(\omega t + \theta)$. The resultant becomes $A_{IN} - A_{IN}^* = \alpha\sin(\omega t + \phi)$, where

$$\alpha = \sqrt{A^2 + 2AB\cos\theta + B^2}, \text{ and}$$

$$\phi = \tan^{-1}\left[\frac{B\sin\theta}{A + B\cos\theta}\right].$$

This shows that neither the amplitude nor the phase of the resultant sine wave are functions of time. In other words, as long as θ and B stay constant, then the measured sine wave will be a scaled and phase-shifted version of the true signal. Thus, the calibration will eliminate all errors caused by the non-ideal nature of the inputs.

The other inputs to the AD6644 are the ENC and ENC* clock signals. These are ECL-level signals that must have minimal jitter. Any jitter in these signals will directly impact the phase and amplitude measurements.

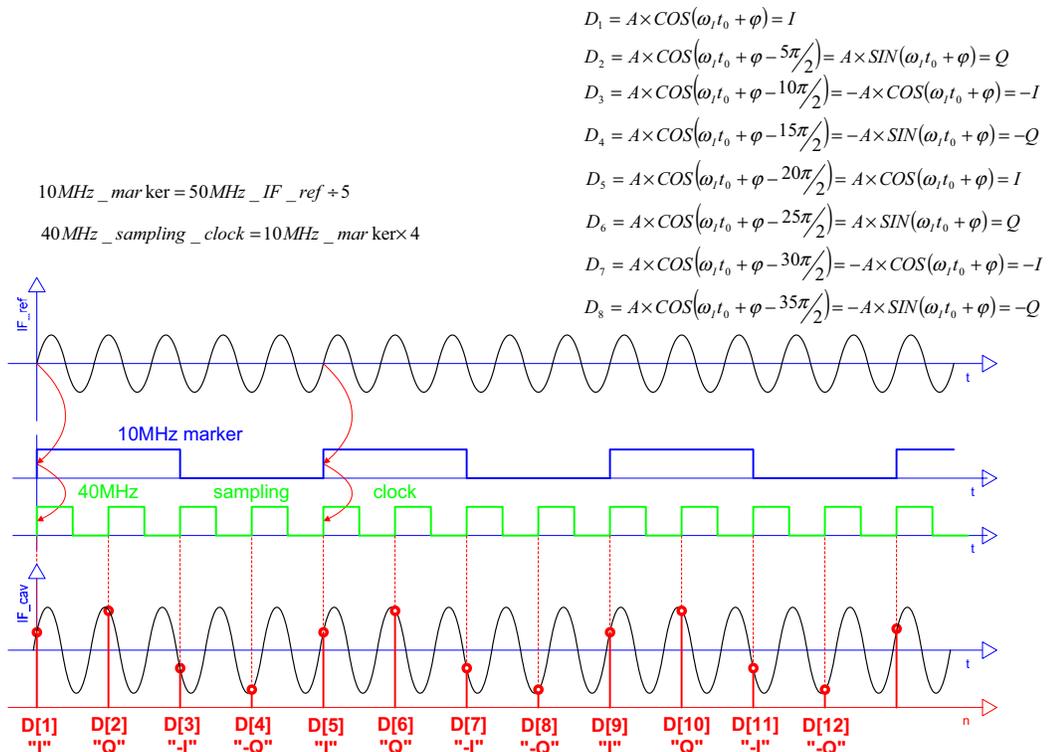
3 I/Q Demodulation

The 50-MHz RF sine wave is sampled by a 40-MHz digital clock. Each time the clock takes a sample, it is at a 90° quadrant of the sine wave. Every fifth sample is synchronized at 0° for both the sine wave and the rising edge of the 40-MHz clock.

This may be easier to understand in terms of time. The 50-MHz sine wave takes 20 ns to run through a 360° cycle. Thus, it takes the sine wave 5 ns to run through each 90° quadrant. The 40-MHz clock takes 25 ns to run through a 360° cycle. Therefore, by the time the 40-MHz clock has run through its 360° cycle, the sine wave has completed its cycle and continued for another 5 ns, or 90° into the next wave.

Looking at it as sequential detection of I and Q data rough sampling, Figure 3-1 helps to explain how sampling a 50-MHz IF signal with a 40-MHz sampling clock provides I and Q data. For this to work with no ambiguity, a fundamental 10-MHz marker, to which the 40- and 50-MHz signals are locked, is used. Figure 3-1 and its accompanying equations were provided by Hengjie Ma of Oak Ridge National Laboratory.

Figure 3-1. I and Q Sampling Explanation



FEATURES

- 300 MHz Internal Clock Rate
- FSK, BPSK, PSK, CHIRP, AM Operation
- Dual Integrated 12-Bit D/A Converters
- Ultrahigh-Speed Comparator, 3 ps RMS Jitter
- Excellent Dynamic Performance: 80 dB SFDR @ 100 MHz (± 1 MHz) A_{OUT}
- 4x to 20x Programmable Reference Clock Multiplier
- Dual 48-Bit Programmable Frequency Registers
- Dual 14-Bit Programmable Phase Offset Registers
- 12-Bit Amplitude Modulation and Programmable Shaped On/Off Keying Function
- Single Pin FSK and BPSK Data Interface
- PSK Capability Via I/O Interface
- Linear or Nonlinear FM Chirp Functions with Single Pin Frequency "Hold" Function
- Frequency-Ramped FSK
- <25 ps RMS Total Jitter in Clock Generator Mode
- Automatic Bidirectional Frequency Sweeping
- SIN(x)/x Correction
- Simplified Control Interface
 - 10 MHz Serial, 2-Wire or 3-Wire SPI-Compatible, or
 - 100 MHz Parallel 8-Bit Programming

3.3 V Single Supply

- Multiple Power-Down Functions
- Single-Ended or Differential Input Reference Clock
- Small 80-Lead LQFP Packaging

APPLICATIONS

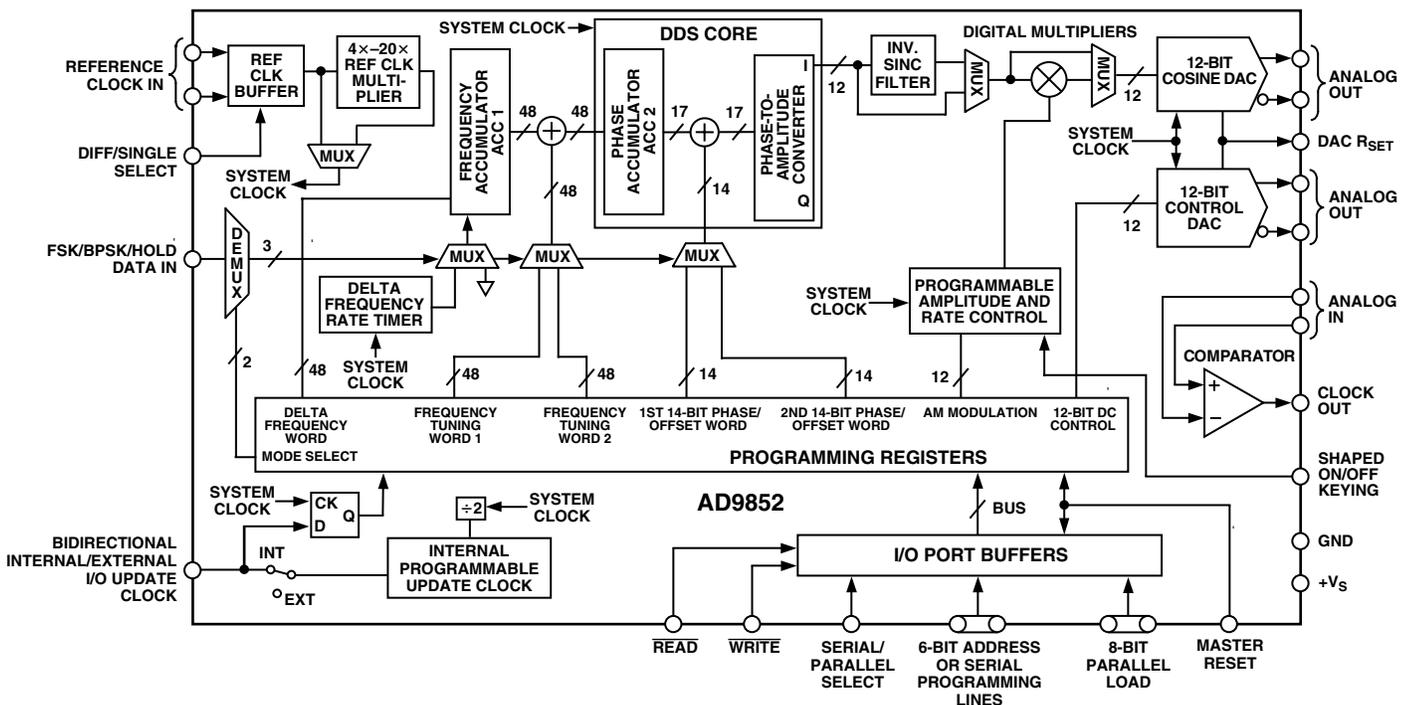
- Agile, L.O. Frequency Synthesis
- Programmable Clock Generator
- FM Chirp Source for Radar and Scanning Systems
- Test and Measurement Equipment
- Commercial and Amateur RF Exciter

GENERAL DESCRIPTION

The AD9852 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with an internal high-speed, high-performance D/A converter to form a digitally programmable agile synthesizer function. When referenced to an accurate clock source, the AD9852 generates a highly stable, frequency-phase-amplitude-programmable cosine output that can be used as an agile L.O. in communications, radar, and many other applications. The AD9852's innovative high-speed DDS core provides 48-bit frequency resolution (1 microHertz tuning resolution with 300 MHz SYSCLK). Maintaining 17 bits assures excellent SFDR. The AD9852's circuit architecture allows the generation of output signals at frequencies up to 150 MHz,

(continued on page 15)

FUNCTIONAL BLOCK DIAGRAM



REV. B

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Parallel I/O Operation	24	To Connect High-Speed Comparator	34
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SPECIFICATIONS

($V_S = 3.3\text{ V} \pm 5\%$, $R_{SET} = 3.9\text{ k}\Omega$ external reference clock frequency = 30 MHz with REFCLK Multiplier enabled at $10\times$ for AD9852ASQ, external reference clock frequency = 20 MHz with REFCLK Multiplier enabled at $10\times$ for AD9852AST unless otherwise noted.)

Parameter	Temp	Test Level	AD9852ASQ			AD9852AST			Unit
			Min	Typ	Max	Min	Typ	Max	
REF CLOCK INPUT CHARACTERISTICS¹									
Internal System Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	20		300	20		200	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
External REF Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	5		75	5		50	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
Duty Cycle	25°C	IV	45	50	55	45	50	55	%
Input Capacitance	25°C	IV		3			3		pF
Input Impedance	25°C	IV		100			100		kΩ
Differential Mode Common-Mode Voltage Range									
Minimum Signal Amplitude ²	25°C	IV	800			800			mV p-p
Common-Mode Range	25°C	IV	1.6	1.75	1.9	1.6	1.75	1.9	V
V_{IH} (Single-Ended Mode)	25°C	IV	2.3			2.3			V
V_{IL} (Single-Ended Mode)	25°C	IV			1			1	V
DAC STATIC OUTPUT CHARACTERISTICS									
Output Update Speed	Full	I			300			200	MSPS
Resolution	25°C	IV		12			12		Bits
Cosine and Control DAC's Full-Scale Output Current	25°C	IV	5	10	20	5	10	20	mA
Gain Error	25°C	I	-6		+2.25	-6		+2.25	% FS
Output Offset	25°C	I			2			2	μA
Differential Nonlinearity	25°C	I		0.3	1.25		0.3	1.25	LSB
Integral Nonlinearity	25°C	I		0.6	1.66		0.6	1.66	LSB
Output Impedance	25°C	IV		100			100		kΩ
Voltage Compliance Range	25°C	I	-0.5		+1.0	-0.5		+1.0	V
DAC DYNAMIC OUTPUT CHARACTERISTICS									
DAC Wideband SFDR									
1 MHz to 20 MHz A_{OUT}	25°C	V		58			58		dBc
20 MHz to 40 MHz A_{OUT}	25°C	V		56			56		dBc
40 MHz to 60 MHz A_{OUT}	25°C	V		52			52		dBc
60 MHz to 80 MHz A_{OUT}	25°C	V		48			48		dBc
80 MHz to 100 MHz A_{OUT}	25°C	V		48			48		dBc
100 MHz to 120 MHz A_{OUT}	25°C	V		48					dBc
DAC Narrowband SFDR									
10 MHz A_{OUT} (± 1 MHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (± 250 kHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (± 50 kHz)	25°C	V		91			91		dBc
41 MHz A_{OUT} (± 1 MHz)	25°C	V		82			82		dBc
41 MHz A_{OUT} (± 250 kHz)	25°C	V		84			84		dBc
41 MHz A_{OUT} (± 50 kHz)	25°C	V		89			89		dBc
119 MHz A_{OUT} (± 1 MHz)	25°C	V		71					dBc
119 MHz A_{OUT} (± 250 kHz)	25°C	V		77					dBc
119 MHz A_{OUT} (± 50 kHz)	25°C	V		83					dBc
Residual Phase Noise									
(A _{OUT} = 5 MHz, Ext. CLK = 30 MHz, REFCLK Multiplier Engaged at $10\times$)									
1 kHz Offset	25°C	V		140			140		dBc/Hz
10 kHz Offset	25°C	V		138			138		dBc/Hz
100 kHz Offset	25°C	V		142			142		dBc/Hz
(A _{OUT} = 5 MHz, Ext. CLK = 300 MHz, REFCLK Multiplier Bypassed)									
1 kHz Offset	25°C	V		142			142		dBc/Hz
10 kHz Offset	25°C	V		148			148		dBc/Hz
100 kHz Offset	25°C	V		152			152		dBc/Hz

AD9852—SPECIFICATIONS (continued)

Parameter	Temp	Test Level	AD9852ASQ			AD9852AST			Unit
			Min	Typ	Max	Min	Typ	Max	
DAC DYNAMIC OUTPUT CHARACTERISTICS (continued)									
Pipeline Delays ^{3, 4, 5}									
DDS Core (Phase Accumulator and Phase-to-Amp Converter)	25°C	IV		33			33	SysClk Cycles	
Frequency Accumulator	25°C	IV		26			26	SysClk Cycles	
Inverse Sinc Filter	25°C	IV		16			16	SysClk Cycles	
Digital Multiplier	25°C	IV		9			9	SysClk Cycles	
DAC	25°C	IV		1			1	SysClk Cycles	
I/O Update Clock (INT Mode)	25°C	IV		2			2	SysClk Cycles	
I/O Update Clock (EXT Mode)	25°C	IV		3			3	SysClk Cycles	
MASTER RESET DURATION	25°C	IV	10			10		SysClk Cycles	
COMPARATOR INPUT CHARACTERISTICS									
Input Capacitance	25°C	V		3			3	pF	
Input Resistance	25°C	IV		500			500	kΩ	
Input Current	25°C	I		±1	±5		±1	±5	
Hysteresis	25°C	IV		10	20		10	20	
COMPARATOR OUTPUT CHARACTERISTICS									
Logic “1” Voltage, High Z Load	Full	VI	3.1			3.1		V	
Logic “0” Voltage, High Z Load	Full	VI			0.16		0.16	V	
Output Power, 50 Ω Load, 120 MHz Toggle Rate	25°C	I	9	11		9	11	dBm	
Propagation Delay	25°C	IV		3			3	ns	
Output Duty Cycle Error ⁶	25°C	I	-10	±1	+10	-10	±1	+10	
Rise/Fall Time, 5 pF Load	25°C	V		2			2	ns	
Toggle Rate, High Z Load	25°C	IV	300	350		300	350	MHz	
Toggle Rate, 50 Ω Load	25°C	IV	375	400		375	400	MHz	
Output Cycle-to-Cycle Jitter ⁷	25°C	IV			4.0			4.0	
COMPARATOR NARROWBAND SFDR ⁸									
10 MHz (±1 MHz)	25°C	V		84			84	dBc	
10 MHz (±250 kHz)	25°C	V		84			84	dBc	
10 MHz (±50 kHz)	25°C	V		92			92	dBc	
41 MHz (±1 MHz)	25°C	V		76			76	dBc	
41 MHz (±250 kHz)	25°C	V		82			82	dBc	
41 MHz (±50 kHz)	25°C	V		89			89	dBc	
119 MHz (±1 MHz)	25°C	V		73			73	dBc	
119 MHz (±250 kHz)	25°C	V		73			73	dBc	
119 MHz (±50 kHz)	25°C	V		83			83	dBc	
CLOCK GENERATOR OUTPUT JITTER ⁸									
5 MHz A _{OUT}	25°C	V		23			23	ps rms	
40 MHz A _{OUT}	25°C	V		12			12	ps rms	
100 MHz A _{OUT}	25°C	V		7			7	ps rms	
PARALLEL I/O TIMING CHARACTERISTICS									
T _{ASU} (Address Setup Time to $\overline{\text{WR}}$ Signal Active)	Full	IV	8.0	7.5		8.0	7.5	ns	
T _{ADHW} (Address Hold Time to $\overline{\text{WR}}$ Signal Inactive)	Full	IV	0			0		ns	
T _{DSU} (Data Setup Time to $\overline{\text{WR}}$ Signal Inactive)	Full	IV	3.0	1.6		3.0	1.6	ns	
T _{DHD} (Data Hold Time to $\overline{\text{WR}}$ Signal Inactive)	Full	IV	0			0		ns	
T _{WRLOW} ($\overline{\text{WR}}$ Signal Minimum Low Time)	Full	IV	2.5	1.8		2.5	1.8	ns	
T _{WRHIGH} ($\overline{\text{WR}}$ Signal Minimum High Time)	Full	IV	7			7		ns	
T _{WR} (Minimum WRITE Time)	Full	IV	10.5			10.5		ns	
T _{ADV} (Address to Data Valid Time)	Full	V	15		15	15		15	
T _{ADHR} (Address Hold Time to $\overline{\text{RD}}$ Signal Inactive)	Full	IV	5			5		ns	
T _{RDLOV} ($\overline{\text{RD}}$ Low-to-Output Valid)	Full	IV			15			15	
T _{RDHOZ} ($\overline{\text{RD}}$ High-to-Data Three-State)	Full	IV			10			10	
SERIAL I/O TIMING CHARACTERISTICS									
T _{PRE} ($\overline{\text{CS}}$ Setup Time)	Full	IV	30			30		ns	
T _{SCLK} (Period of Serial Data Clock)	Full	IV	100			100		ns	
T _{DSU} (Serial Data Setup Time)	Full	IV	30			30		ns	
T _{SCLKPWH} (Serial Data Clock Pulsewidth High)	Full	IV	40			40		ns	
T _{SCLKPWL} (Serial Data Clock Pulsewidth Low)	Full	IV	40			40		ns	
T _{DHLD} (Serial Data Hold Time)	Full	IV	0			0		ns	
T _{DV} (Data Valid Time)	Full	V		30			30	ns	

Parameter	Temp	Test Level	AD9852ASQ			AD9852AST			Unit
			Min	Typ	Max	Min	Typ	Max	
SERIAL I/O TIMING CHARACTERISTICS (continued)									
CMOS LOGIC INPUTS ⁹									
Logic "1" Voltage	25°C	I	2.2			2.2			V
Logic "0" Voltage	25°C	I			0.8			0.8	V
Logic "1" Current	25°C	IV			±5			±12	µA
Logic "0" Current	25°C	IV			±5			±12	µA
Input Capacitance	25°C	V		3			3		pF
POWER SUPPLY ¹⁰									
+V _S Current ¹¹	25°C	I		815	922		585	660	mA
+V _S Current ¹²	25°C	I		640	725		465	520	mA
+V _S Current ¹³	25°C	I		585	660		425	475	mA
P _{DISS} ¹¹	25°C	I		2.70	3.20		1.93	2.39	W
P _{DISS} ¹²	25°C	I		2.12	2.52		1.53	1.81	W
P _{DISS} ¹³	25°C	I		1.93	2.29		1.40	1.65	W
P _{DISS} Power-Down Mode	25°C	I		1	50		1	50	mW

NOTES

- ¹The reference clock inputs are configured to accept a 1 V p-p (typical) dc offset square or sine waves centered at one-half the applied V_{DD} or a 3 V TTL-level pulse input.
- ²An internal 800 mV p-p differential voltage swing equates to 400 mV p-p applied to both REFCLK input pins.
- ³Pipeline delays of each individual block are fixed; however, if the eight top MSBs of a tuning word are all zeros, the delay will appear longer. This is due to insufficient phase accumulation per a system clock period to produce enough LSB amplitude to the D/A converter.
- ⁴If a feature such as inverse sinc, which has 16 pipeline delays, can be bypassed, the total delay will be reduced by that amount.
- ⁵The I/O Update CLK transfers data from the I/O Port Buffers to the Programming Registers. This transfer takes system clocks to perform.
- ⁶Change in duty cycle from 1 MHz to 100 MHz with 1 V p-p sine wave input and 0.5 V threshold.
- ⁷Represents comparator's inherent cycle-to-cycle jitter contribution. Input signal is a 1 V, 40 MHz square wave. Measurement device Wavecrest DTS – 2075.
- ⁸Comparator input originates from analog output section via external 7-pole elliptic LPF. Single-ended input, 0.5 V p-p. Comparator output terminated in 50 Ω.
- ⁹Avoid overdriving digital inputs. (Refer to equivalent circuits in Figure 1.)
- ¹⁰Simultaneous operation at the maximum ambient temperature of 85°C and the maximum internal clock frequency of 200 MHz for the 80-lead LQFP, or 300 MHz for the thermally-enhanced 80-lead LQFP may cause the maximum die junction temperature of 150°C to be exceeded. Refer to the section titled Power Dissipation and Thermal Considerations for derating and thermal management information.
- ¹¹All functions engaged.
- ¹²All functions except inverse sinc engaged.
- ¹³All functions except inverse sinc and digital multipliers engaged.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

- I. 100% Production Tested.
- III. Sample Tested Only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ABSOLUTE MAXIMUM RATINGS*

Maximum Junction Temperature	150°C
V _S	4 V
Digital Inputs	-0.7 V to +V _S
Digital Output Current	5 mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Maximum Clock Frequency (ASQ)	300 MHz
Maximum Clock Frequency (AST)	200 MHz
θ _{JA} (ASQ)	16°C/W
θ _{JC} (ASQ)	2°C/W
θ _{JA} (AST)	38°C/W

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9852ASQ	-40°C to +85°C	Thermally Enhanced 80-Lead LQFP	SQ-80
AD9852AST	-40°C to +85°C	80-Lead LQFP	ST-80
AD9852/PCB	0°C to 70°C	Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9852 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

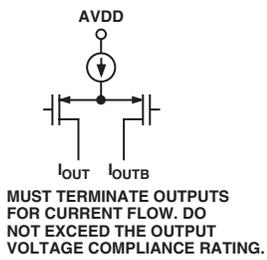
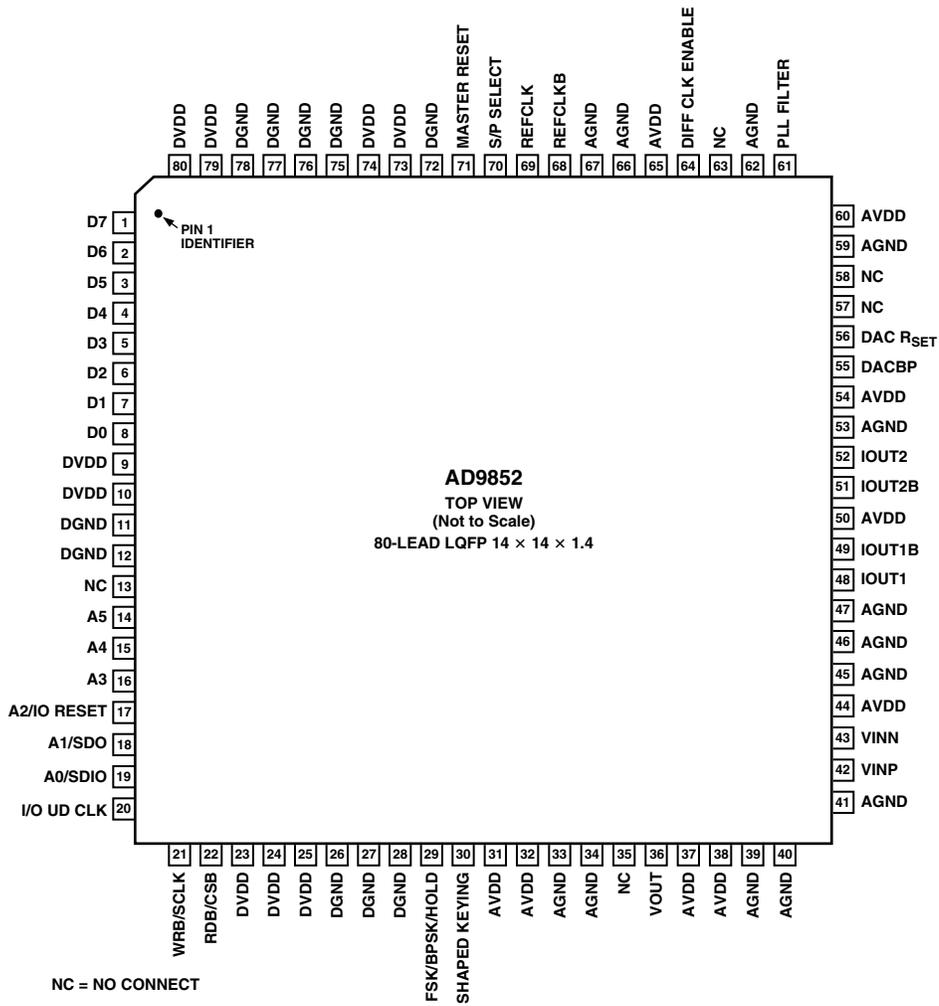


PIN FUNCTION DESCRIPTIONS

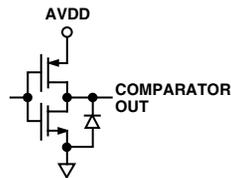
Pin Number	Mnemonic	Function
1–8	D7–D0	Eight-Bit Bidirectional Parallel Programming Data Inputs. Used only in parallel programming mode.
9, 10, 23, 24, 25, 73, 74, 79, 80	DVDD	Connections for the Digital Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND
11, 12, 26, 27, 28, 72, 75, 76, 77, 78	DGND	Connections for Digital Circuitry Ground Return. Same potential as AGND.
13, 35, 57, 58, 63	NC	No Internal Connection
14–19	A5–A0	Six-Bit Parallel Address Inputs for Program Registers. Used only in parallel programming mode. A0, A1, and A2 have a second function when the serial programming mode is selected. See immediately below.
17	A2/IO RESET	Allows an IO RESET of the serial communications bus that is unresponsive due to improper programming protocol. Resetting the serial bus in this manner does not affect previous programming, nor does it invoke the “default” programming values seen in the Table IV. Active HIGH.
18	A1/SDO	Unidirectional Serial Data Output for Use in 3-Wire Serial Communication Mode.
19	A0/SDIO	Bidirectional Serial Data Input/Output for Use in 2-Wire Serial Communication Mode.
20	I/O UD CLK	Bidirectional I/O Update CLK. Direction is selected in control register. If selected as an input, a rising edge will transfer the contents of the I/O Port Buffers to the Programming Registers. If I/O UD is selected as an output (Default), an output pulse (low to high) of eight system clock cycle duration indicates that an internal frequency update has occurred.
21	WRB/SCLK	Write Parallel Data to I/O Port Buffers. Shared function with SCLK. Serial clock signal associated with the serial programming bus. Data is registered on the rising edge. This pin is shared with WRB when the parallel mode is selected. Mode dependent on Pin 70 (S/P Select).
22	RDB/CSB	Read Parallel Data from Programming Registers. Shared function with CSB. Chip-select signal associated with the serial programming bus. Active LOW. This pin is shared with RDB when the parallel mode is selected.
29	FSK/BPSK/ HOLD	Multifunction Pin According to the Mode of Operation Selected in the Programming Control Register. If in the FSK mode, logic low selects F1, logic high selects F2. If in the BPSK mode, logic low selects Phase 1, logic high selects Phase 2. If in the Chirp mode, logic high engages the HOLD function causing the frequency accumulator to halt at its current location. To resume or commence Chirp, logic low is asserted.
30	SHAPED KEYING	Must First Be Selected in the Programming Control Register to Function. A logic high will cause the Cosine DAC outputs to ramp up from zero-scale to full-scale amplitude at a pre-programmed rate. Logic low causes the full-scale output to ramp down to zero-scale at the preprogrammed rate.
31, 32, 37, 38, 44, 50, 54, 60, 65	AVDD	Connections for the Analog Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND.
33, 34, 39, 40, 41, 45, 46, 47, 53, 59, 62, 66, 67	AGND	Connections for Analog Circuitry Ground Return. Same potential as DGND.
36	VOUT	Internal High-Speed Comparator’s Noninverted Output Pin. Designed to drive 10 dBm to 50 Ω load as well as standard CMOS logic levels.
42	VINP	Voltage Input Positive. The internal high-speed comparator’s noninverting input.
43	VINN	Voltage Input Negative. The internal high-speed comparator’s inverting input.
48	IOUT1	Unipolar Current Output of the Cosine DAC. (Refer to Figure 1.)
49	IOUT1B	Complementary Unipolar Current Output of the Cosine DAC
51	IOUT2B	Complementary Unipolar Current Output of the Control DAC
52	IOUT2	Unipolar Current Output of the Control DAC

Pin Number	Mnemonic	Function
55	DACBP	Common Bypass Capacitor Connection for Both DACs. A 0.01 μ F chip cap from this pin to AVDD improves harmonic distortion and SFDR slightly. No connect is permissible (slight SFDR degradation).
56	DAC R _{SET}	Common Connection for Both DACs to Set the Full-Scale Output Current. $R_{SET} = 39.9/I_{OUT}$. Normal R _{SET} range is from 8 k Ω (5 mA) to 2 k Ω (20 mA).
61	PLL FILTER	This pin provides the connection for the external zero compensation network of the REFCLK Multiplier's PLL loop filter. The zero compensation network consists of a 1.3 k Ω resistor in series with a 0.01 μ F capacitor. The other side of the network should be connected to AVDD as close as possible to Pin 60. For optimum phase noise performance, the REFCLK Multiplier can be bypassed by setting the "Bypass PLL" bit in control register 1E.
64	DIFF CLK ENABLE	Differential REFCLK Enable. A high level of this pin enables the differential clock inputs, REFCLK and REFCLKB (Pins 69 and 68 respectively).
68	REFCLKB	The Complementary (180 Degrees Out-of-Phase) Differential Clock Signal. User should tie this pin high or low when single-ended clock mode is selected. Same signal levels as REF CLK.
69	REFCLK	Single-Ended (CMOS logic levels required) Reference Clock Input or One of Two Differential Clock Signals. In Differential Ref Clock mode, both inputs can be CMOS logic levels or have greater than 400 mV p-p square or sine waves centered about 1.6 V dc.
70	S/P SELECT	Selects Between Serial Programming Mode (Logic LOW) and Parallel Programming Mode (Logic HIGH).
71	MASTER RESET	Initializes the serial/parallel programming bus to prepare for user programming; sets programming registers to a "do-nothing" state defined by the default values seen in Table IV. Active on logic high. Asserting MASTER RESET is essential for proper operation upon power-up.

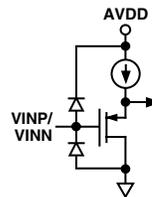
PIN CONFIGURATION



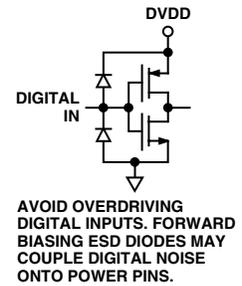
a. DAC Outputs



b. Comparator Output



c. Comparator Input

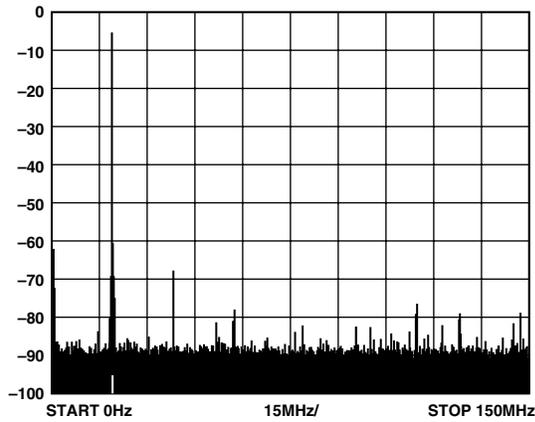


d. Digital Input

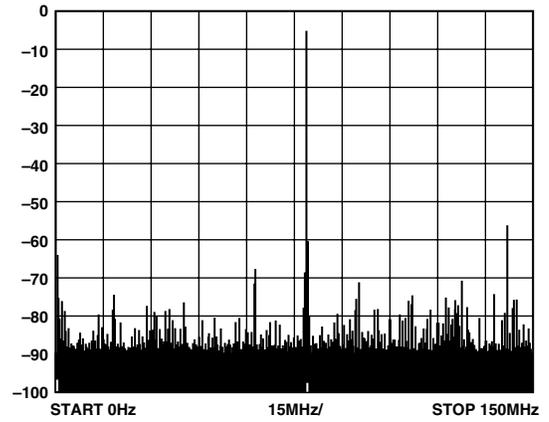
Figure 1. Equivalent Input and Output Circuits

Typical Performance Characteristics—AD9852

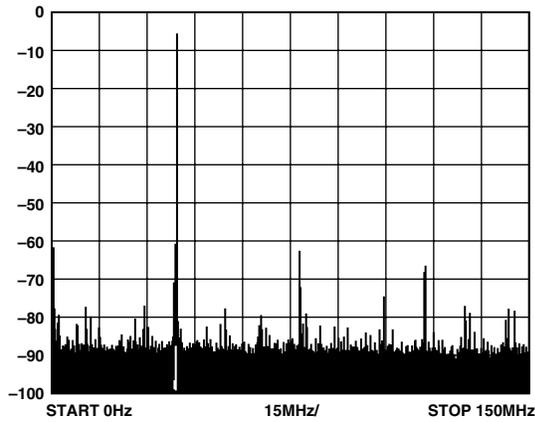
TPCs 1–6 indicate the wideband harmonic distortion performance of the AD9852 from 19.1 MHz to 119.1 MHz Fundamental Output, Reference Clock = 30 MHz, REFCLK Multiplier = 10. Each graph plotted from 0 MHz to 150 MHz (Nyquist).



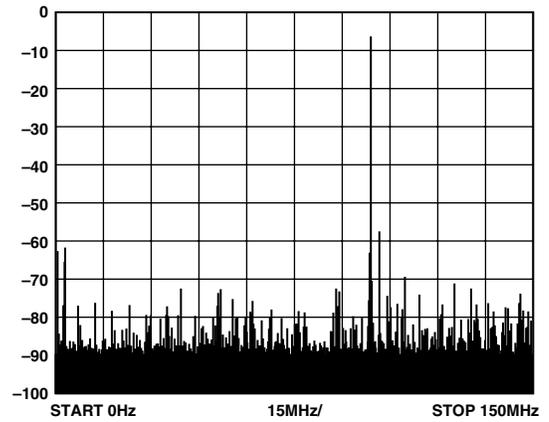
TPC 1. Wideband SFDR, 19.1 MHz



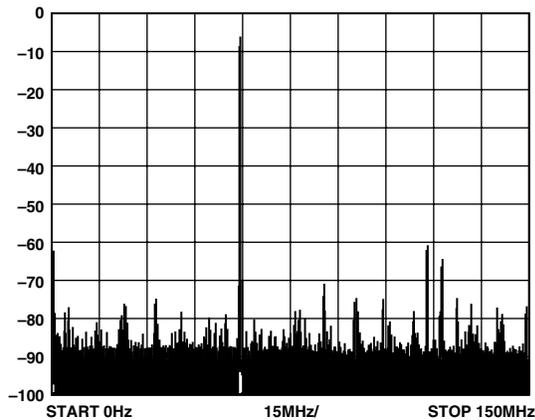
TPC 4. Wideband SFDR, 79.1 MHz



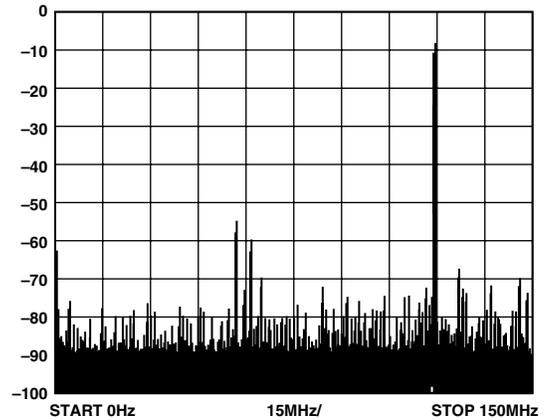
TPC 2. Wideband SFDR, 39.1 MHz



TPC 5. Wideband SFDR, 99.1 MHz



TPC 3. Wideband SFDR, 59.1 MHz

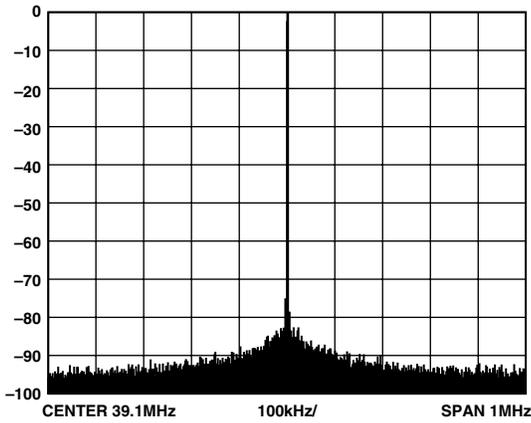


TPC 6. Wideband SFDR, 119.1 MHz

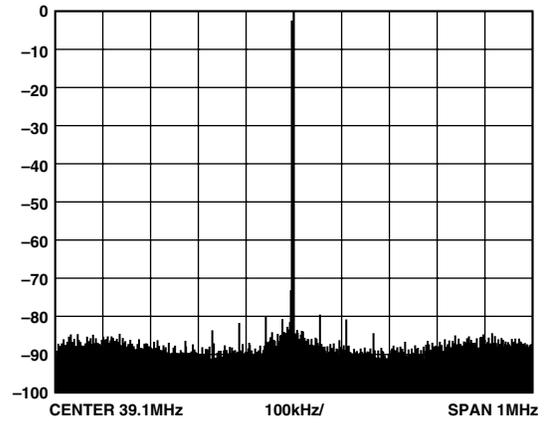
AD9852

TPCs 7–10 show the trade-off in elevated noise floor, increased phase noise, and discrete spurious energy when the internal REFCLK Multiplier circuit is engaged. Plots with wide (1 MHz) and narrow (50 kHz) spans are shown.

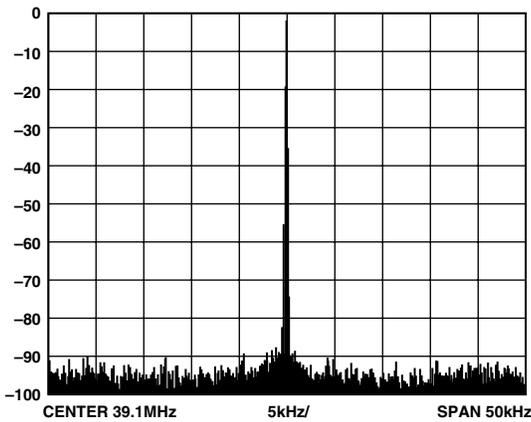
Compare the noise floor of TPCs 8 and 10 to TPCs 11 and 12. The improvement seen in TPCs 8 and 10 is a direct result of sampling the fundamental at a higher rate. Sampling at a higher rate spreads the quantization noise of the DAC over a wider bandwidth, which effectively lowers the noise floor.



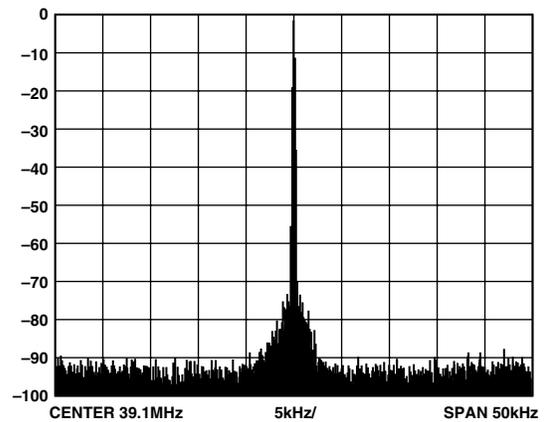
TPC 7. Narrowband SFDR, 39.1 MHz, 1 MHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed



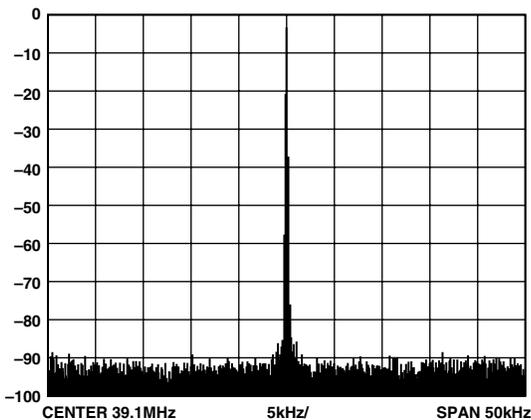
TPC 10. Narrowband SFDR, 39.1 MHz, 1 MHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10x



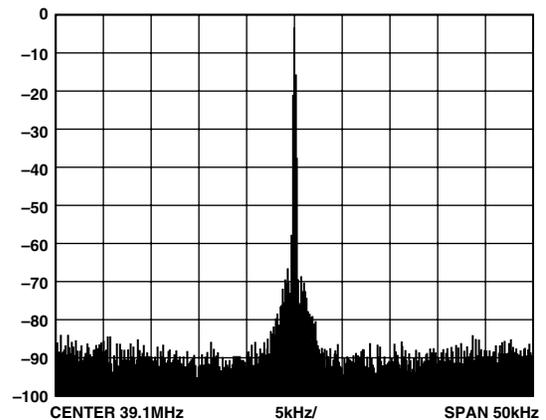
TPC 8. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed



TPC 11. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10x

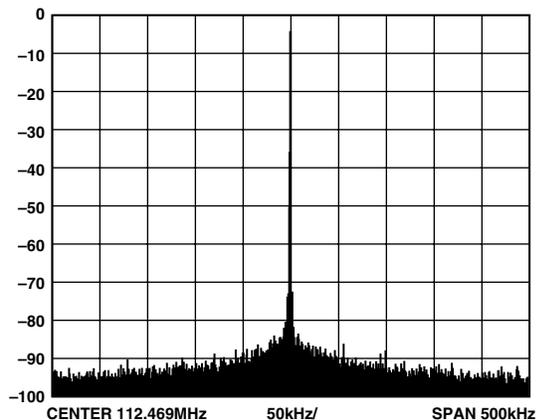


TPC 9. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 100 MHz REFCLK with REFCLK Multiplier Bypassed

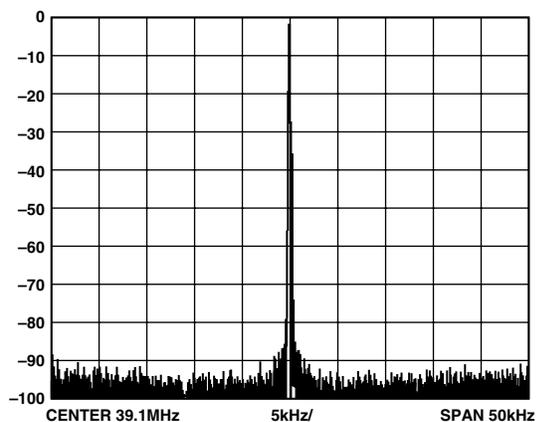


TPC 12. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 10 MHz REFCLK with REFCLK Multiplier = 10x

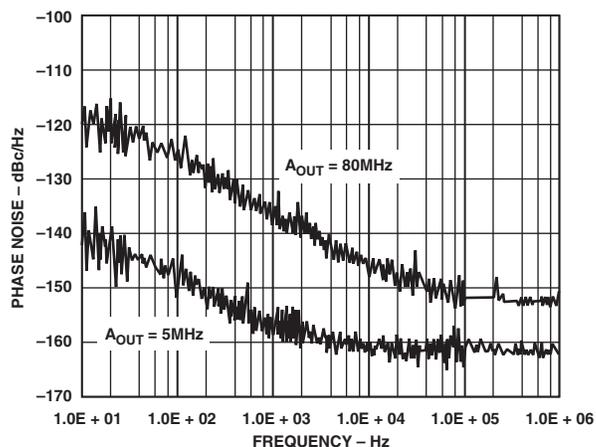
TPC 14 shows the narrowband performance of the AD9852 when operating with a 20 MHz reference clock and the REFCLK Multiplier enabled at 10× vs. a 200 MHz reference clock with REFCLK Multiplier bypassed.



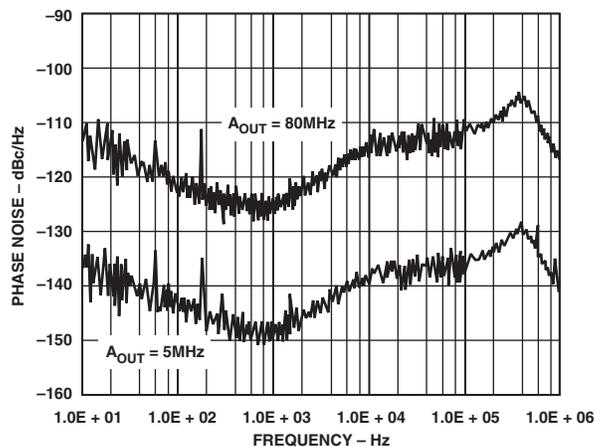
TPC 13. A slight change in tuning word yields dramatically better results. 112.469 MHz with all spurs shifted out-of-band. REFCLK is 300 MHz.



TPC 14. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 200 MHz REFCLK with REFCLK Multiplier Bypassed

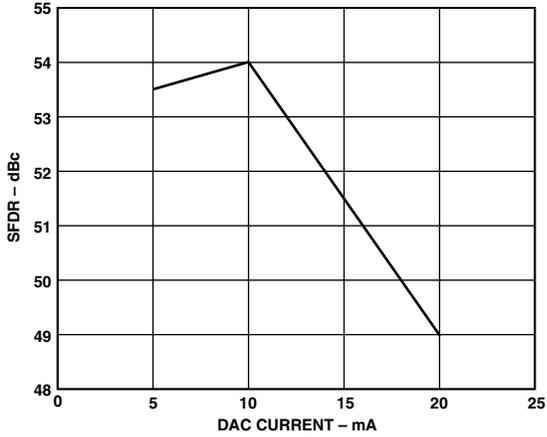


TPC 15a. Residual Phase Noise, 300 MHz REFCLK with REFCLK Multiplier Bypassed

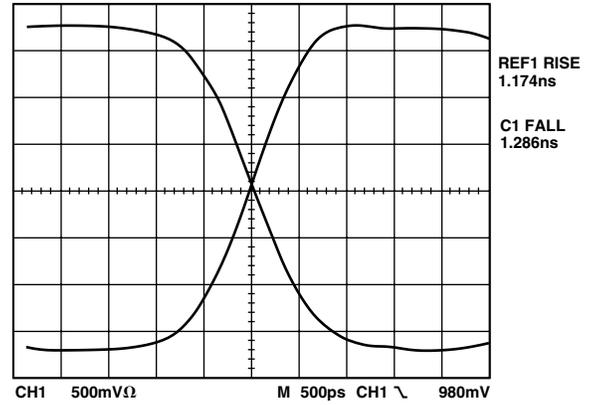


TPC 15b. Residual Phase Noise, 30 MHz REFCLK with REFCLK Multiplier = 10×

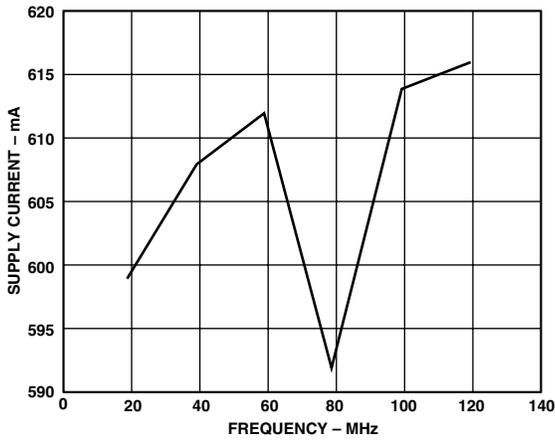
AD9852



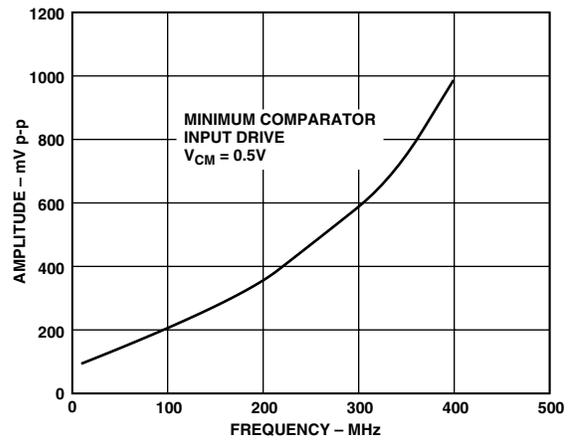
TPC 16. SFDR vs. DAC Current, 59.1 A_{OUT}, 300 MHz REFCLK with REFCLK Multiplier Bypassed



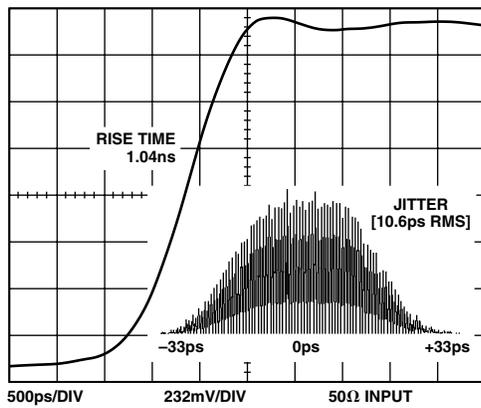
TPC 19. Comparator Rise/Fall Times



TPC 17. Supply Current vs. Output Frequency; Variation Is Minimal as a Percentage and Heavily Dependent on Tuning Word



TPC 20. Comparator Toggle Voltage Requirement



TPC 18. Typical Comparator Output Jitter, 40 MHz A_{OUT}, 300 MHz REFCLK with REFCLK Multiplier Bypassed

TYPICAL APPLICATIONS

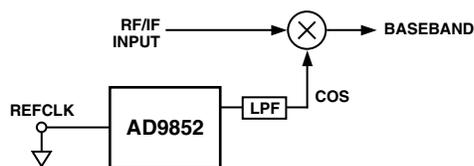


Figure 2. Synthesized L.O. Application for the AD9852

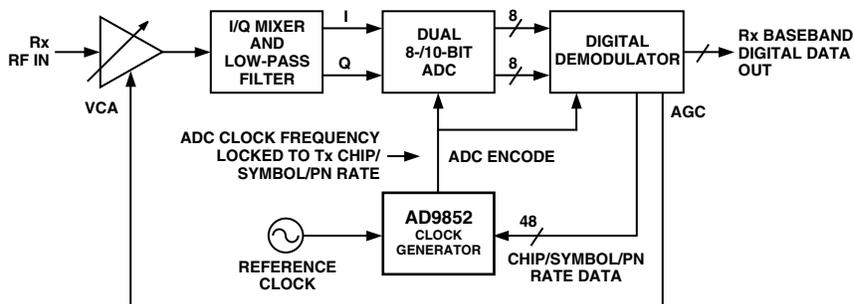


Figure 3. Chip Rate Generator in Spread Spectrum Application

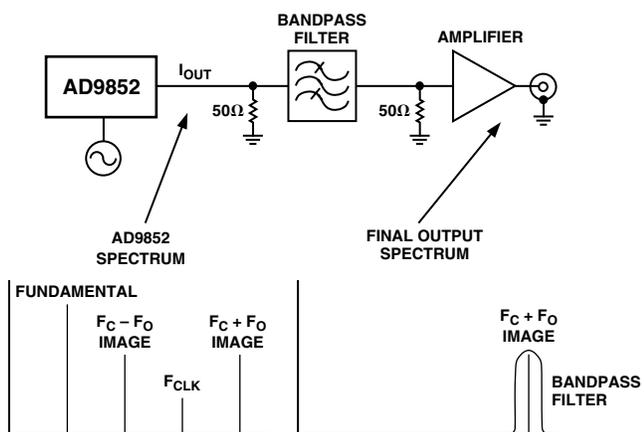


Figure 4. Using an Aliased Image to Generate a High Frequency

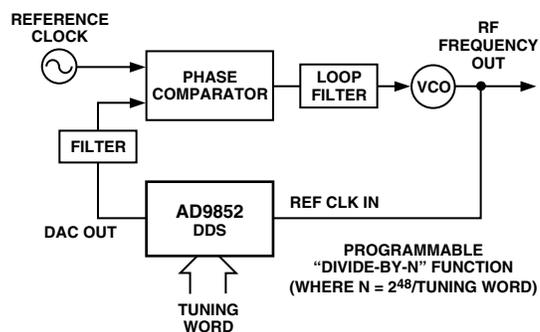


Figure 5. Programmable "Fractional Divide-by-N" Synthesizer

AD9852

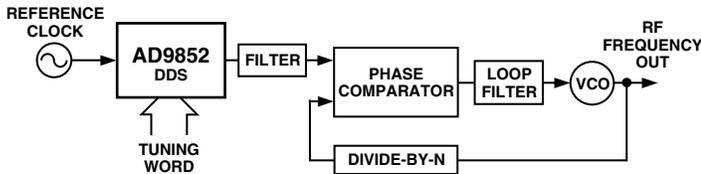


Figure 6. Agile High-Frequency Synthesizer

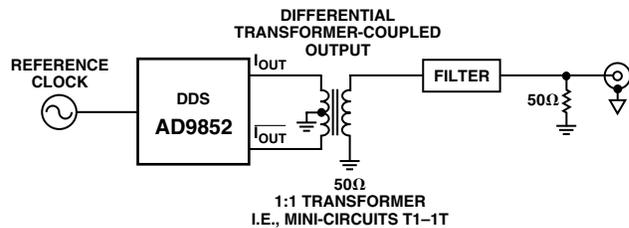


Figure 7. Differential Output Connection for Reduction of Common-Mode Signals

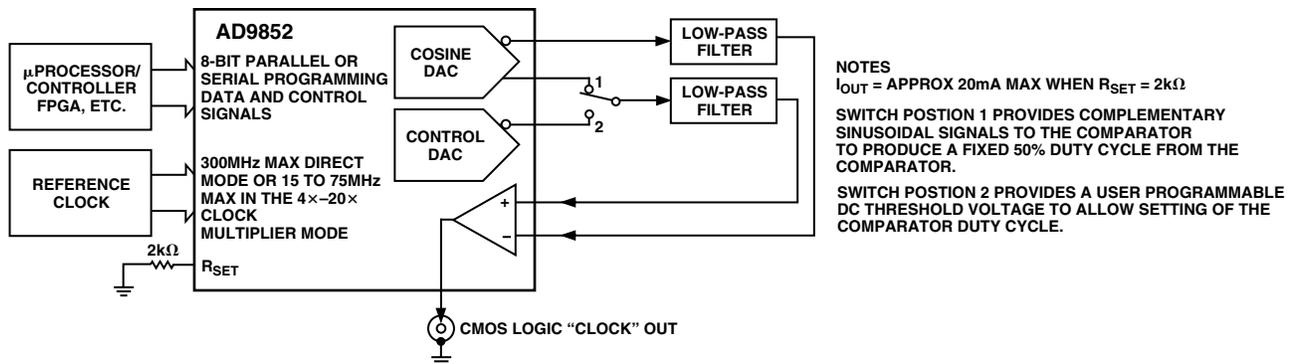


Figure 8. Frequency Agile Clock Generator Applications for the AD9852

(continued from page 1)

which can be digitally tuned at a rate of up to 100 million new frequencies per second. The (externally filtered) cosine wave output can be converted to a square wave by the internal comparator for agile clock generator applications. The device provides two 14-bit phase registers and a single pin for BPSK operation. For higher order PSK operation, the user may use the I/O Interface for phase changes. The 12-bit cosine DAC, coupled with the innovative DDS architecture, provides excellent wide-band and narrow-band output SFDR. When configured with the comparator, the 12-bit control DAC facilitates static duty cycle control in the high-speed clock generator applications. The 12-bit digital multiplier permits programmable amplitude modulation, shaped on/off keying and precise amplitude control of the cosine DAC output. Chirp functionality is also included which facilitates wide bandwidth frequency sweeping applications. The AD9852's programmable $4\times$ – $20\times$ REFCLK multiplier circuit generates the 300 MHz system clock internally from a lower frequency external reference clock. This saves the user the expense and difficulty of implementing a 300 MHz system clock source. Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of “ramped” FSK are supported. The AD9852 uses advanced 0.35 micron CMOS technology to provide this high level of functionality on a single 3.3 V supply.

The AD9852 is available in a space-saving 80-lead LQFP surface mount package and a thermally enhanced 80-lead LQFP package. The AD9852 is pin-for-pin compatible with the AD9854 single-tone synthesizer. It is specified to operate over the extended industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

OVERVIEW

The AD9852 digital synthesizer is a highly flexible device that will address a wide range of applications. The device consists of an NCO with 48-bit phase accumulator, programmable reference clock multiplier, inverse sinc filter, digital multiplier, two 12-bit/300 MHz DACs, high-speed analog comparator, and interface logic. This highly integrated device can be configured to serve as a synthesized LO, agile clock generator, and FSK/BPSK modulator. The theory of operation of the functional blocks of the device, and a technical description of the signal flow through a DDS device, can be found in a tutorial from Analog Devices called “A Technical Tutorial on Digital Signal Synthesis.” This tutorial is available on CD-ROM and information on obtaining it can be found at the Analog Devices DDS website at www.analog.com/dds. The tutorial also provides basic applications information for a variety of digital synthesis implementations. The DDS background subject matter is not covered in this data sheet; the functions and features of the AD9852 will be individually discussed herein.

DESCRIPTION OF AD9852 MODES OF OPERATION

There are five programmable modes of operation of the AD9852. Selecting a mode requires that three bits in the Control Register (parallel address 1F hex) be programmed as follows in Table I.

Table I. Mode Selection Table

Mode 2	Mode 1	Mode 0	Result
0	0	0	SINGLE-TONE
0	0	1	FSK
0	1	0	RAMPED FSK
0	1	1	CHIRP
1	0	0	BPSK

In each mode, engaging certain functions may not be permitted. Shown in Table II is a listing of some important functions and their availability for each mode.

Single-Tone (Mode 000)

This is the default mode when master reset is asserted. It may also be accessed by being user-programmed into the control register. The Phase Accumulator, responsible for generating an output frequency, is presented with a 48-bit value from Frequency Tuning Word 1 registers whose default values are zero. Default values from the remaining applicable registers will further define the single-tone output signal qualities.

The default values after a master reset configure the device with an output signal of 0 Hertz, 0 phase. Upon power-up and reset, the output from both DACs will be a dc value equal to the midscale output current. This is the default mode amplitude setting of zero. Refer to the digital multiplier section for further explanation of the output amplitude control. It will be necessary to program all or some of the 28 program registers to realize a user-defined output signal.

Figure 9 graphically shows the transition from the default condition (0 Hz) to a user-defined output frequency (F1).

As with all Analog Devices DDSs, the value of the frequency tuning word is determined using the following equation:

$$FTW = (\text{Desired Output Frequency} \times 2^N) / \text{SYSCLK}$$

Where N is the phase accumulator resolution (48 bits in this instance), frequency is expressed in Hertz, and the FTW,

Frequency Tuning Word, is a decimal number. Once a decimal number has been calculated, it must be rounded to an integer and then converted to binary format—a series of 48 binary-weighted 1s or 0s. The fundamental sine wave DAC output frequency range is from dc to 1/2 SYSCLK.

Changes in frequency are phase-continuous, which means that the first sampled phase value of the new frequency will be referenced in time from the last sampled phase value of the previous frequency.

The 14-bit phase register adjusts the phase of the cosine DAC's output.

The single-tone mode allows the user to control the following signal qualities:

- Output Frequency to 48-Bit Accuracy
- Output Amplitude to 12-Bit Accuracy
 - Fixed, User-Defined, Amplitude Control
 - Variable, Programmable Amplitude Control
 - Automatic, Programmable, Single-Pin-Controlled, “Shaped On/Off Keying”
- Output Phase to 14-Bit Accuracy

Furthermore, all of these qualities can be changed or modulated via the 8-bit parallel programming port at a 100 MHz parallel-byte rate, or at a 10 MHz serial rate. Incorporating this attribute will permit FM, AM, PM, FSK, PSK, ASK operation in the single-tone mode.

Unramped FSK (Mode 001)

When selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word registers 1 and 2 and the logic level of Pin 29 (FSK/BPSK/HOLD). A logic low on Pin 29 chooses F1 (frequency tuning word 1, parallel address 4–9 hex) and a logic high chooses F2 (frequency tuning word 2, parallel register address A–F hex). Changes in frequency are phase-continuous and are internally coincident with the FSK data pin (29); however, there is deterministic pipeline delay between the FSK data signal and the DAC Output. (Please refer to pipeline delays in specification table.)

The unramped FSK mode, Figure 10, is representative of traditional FSK, RTTY (Radio Teletype) or TTY (Teletype) transmission of digital data. FSK is a very reliable means of digital communication; however, it makes inefficient use of the bandwidth in the RF Spectrum. Ramped FSK in Figure 11 is a method of conserving the bandwidth.

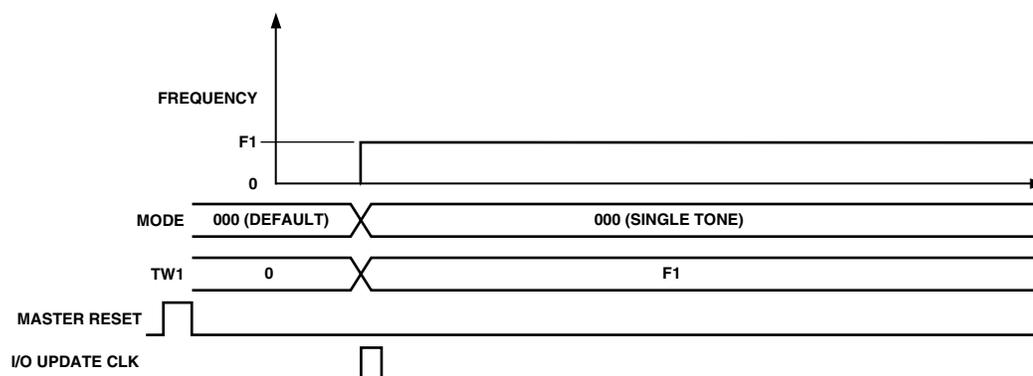


Figure 9. Default State to User-Defined Output Transition

Table II. Function Availability vs. Mode of Operation

Mode	Phase Adjust 1	Phase Adjust 2	Single-Pin FSK/BPSK or HOLD	Single-Pin Shaped-Keying	Phase Offset or Modulation	Amplitude Control or Modulation	Inverse SINC Filter	Frequency Tuning Word 1	Frequency Tuning Word 2	Automatic Frequency Sweep
Single-Tone	✓	X	X	✓	✓	✓	✓	✓	X	X
FSK	✓	X	✓	✓	✓	✓	✓	✓	✓	X
Ramped FSK	✓	X	✓	✓	✓	✓	✓	✓	✓	✓
CHIRP	✓	X	✓	✓	✓	✓	✓	✓	X	✓
BPSK	✓	✓	✓	✓	X	✓	✓	✓	X	X

Ramped FSK (Mode 010)

A method of FSK whereby changes from F1 to F2 are not instantaneous but, instead, are accomplished in a frequency sweep or “ramped” fashion. The “ramped” notation implies that the sweep is linear. While linear sweeping or frequency ramping is easily and automatically accomplished, it is only one of many possibilities. Other frequency transition schemes may be implemented by changing the ramp rate and ramp step size on-the-fly, in piecewise fashion.

Frequency ramping, whether linear or nonlinear, necessitates that many intermediate frequencies between F1 and F2 will be output in addition to the primary F1 and F2 frequencies. Figures 11 and 12 graphically depict the frequency versus time characteristics of a linear ramped FSK signal.

NOTE: In ramped FSK mode, the Delta Frequency (DFW) is required to be programmed as a positive two’s complement value. Another requirement is that the lowest frequency (F1) be programmed in the Frequency Tuning Word 1 register.

The purpose of ramped FSK is to provide better bandwidth containment than traditional FSK by replacing the instantaneous frequency changes with more gradual, user-defined frequency changes. The dwell time at F1 and F2 can be equal to or much greater than the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of intermediate frequencies and time spent at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency into F2 registers.

Several registers must be programmed to instruct the DDS regarding the resolution of intermediate frequency steps (48 bits) and the time spent at each step (20 bits). Furthermore, the CLR ACC1 bit in the control register should be toggled (low-high-low) prior to operation to assure that the frequency accumulator is starting from an “all zeros” output condition. For piecewise, nonlinear frequency transitions, it is necessary to reprogram the registers *while* the frequency transition is in progress to affect the desired response.

Parallel register addresses 1A–1C hex comprise the 20-bit “Ramp Rate Clock” registers. This is a countdown counter that outputs a single pulse whenever the count reaches zero. The counter is activated any time a logic level change occurs on FSK input Pin 29. This counter is run at the System Clock Rate, 300 MHz maximum. The time period between each output pulse is given as

$$(N + 1) = (\text{SYSTEM CLOCK PERIOD})$$

where *N* is the 20-bit ramp rate clock value programmed by the user. Allowable range of *N* is from 1 to $(2^{20} - 1)$. The output of this counter clocks the 48-bit Frequency Accumulator shown below in Figure 13. The Ramp Rate Clock determines the amount of time spent at each intermediate frequency between F1 and F2. The counter stops automatically when the destination frequency is achieved. The “dwell time” spent at F1 and F2 is determined by the duration that the FSK input, Pin 29, is held high or low after the destination frequency has been reached.

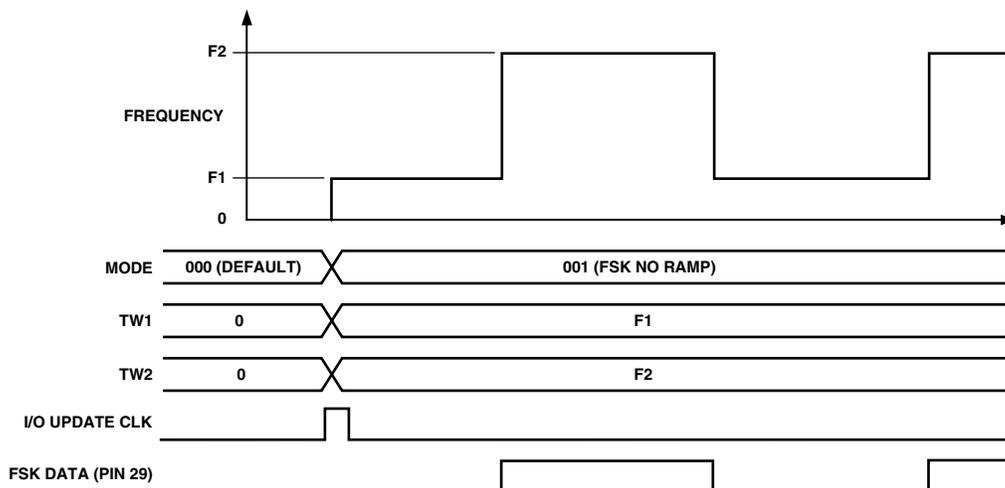


Figure 10. Traditional FSK Mode

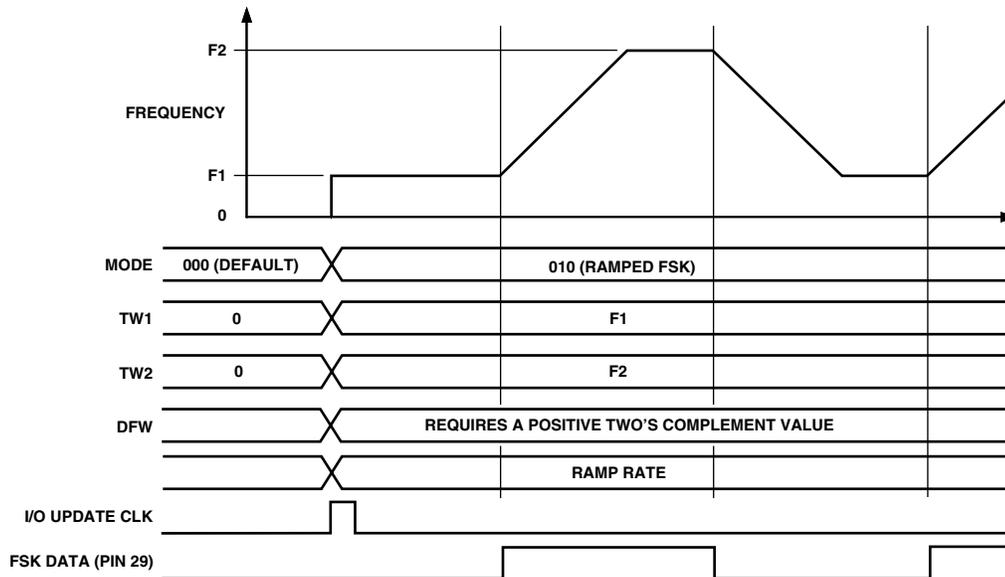


Figure 11. Ramped FSK Mode

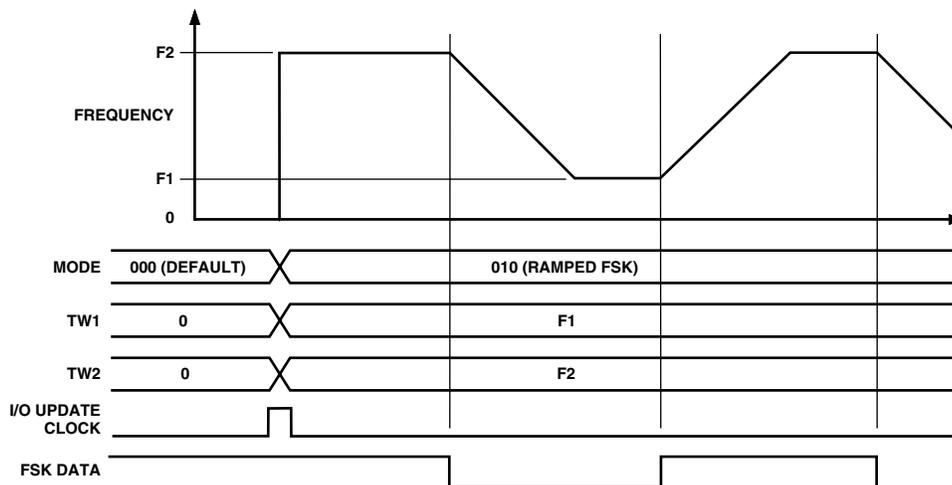


Figure 12. Ramped FSK Mode

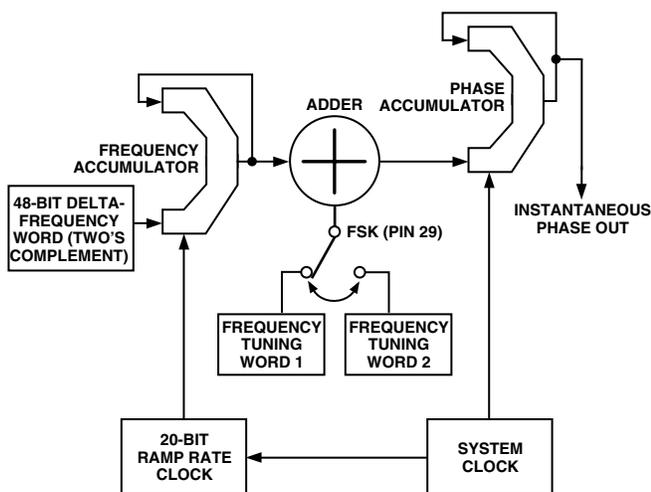


Figure 13. Block Diagram of Ramped FSK Function

Parallel register addresses 10–15 hex comprise the 48-bit, two's complement, "Delta Frequency Word" registers. This 48-bit word is accumulated (added to the accumulator's output) every time it receives a clock pulse from the ramp rate counter. The output of this accumulator is then added to or subtracted from the F1 or F2 frequency word, which is then fed to the input of the 48-bit Phase Accumulator that forms the numerical phase steps for the sine and cosine wave outputs. In this fashion, the output frequency is ramped up and down in frequency, according to the logic-state of Pin 29. The rate at which this happens is a function of the 20-bit ramp rate clock. Once the destination frequency is achieved, the ramp rate clock is stopped, which halts the frequency accumulation process.

Generally speaking, the Delta Frequency Word will be a much smaller value compared to that of the F1 or F2 tuning word. For example, if F1 and F2 are 1 kHz apart at 13 MHz, the Delta Frequency Word might be only 25 Hz.

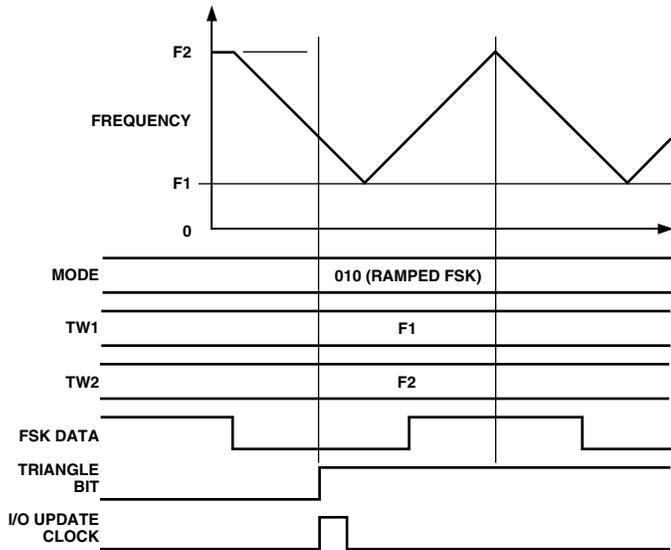


Figure 14. Effect of Triangle Bit in Ramped FSK Mode

Figure 15 shows that premature toggling causes the ramp to immediately reverse itself and proceed at the same rate and resolution back to originating frequency.

The control register contains a Triangle bit at parallel register address 1F hex. Setting this bit high in Mode 010 causes an *automatic* ramp-up and ramp-down between F1 and F2 to occur without having to toggle Pin 29 as shown in Figure 14. In fact, the logic state of Pin 29 has no effect once the Triangle bit is set high. This function uses the ramp-rate clock time period and the delta-frequency-word step size to form a *continuously* sweeping linear ramp from F1 to F2 and back to F1 with equal dwell times at every frequency. Using this function, one can automatically sweep between any two frequencies from dc to Nyquist.

In the ramped FSK mode, with the triangle bit set high, an automatic frequency sweep will begin at either F1 or F2, according to the logic level on Pin 29 (FSK input pin) when the triangle bit's rising edge occurs as shown in Figure 16. If the FSK data bit had been high instead of low, F2, rather than F1, would have been chosen as the start frequency.

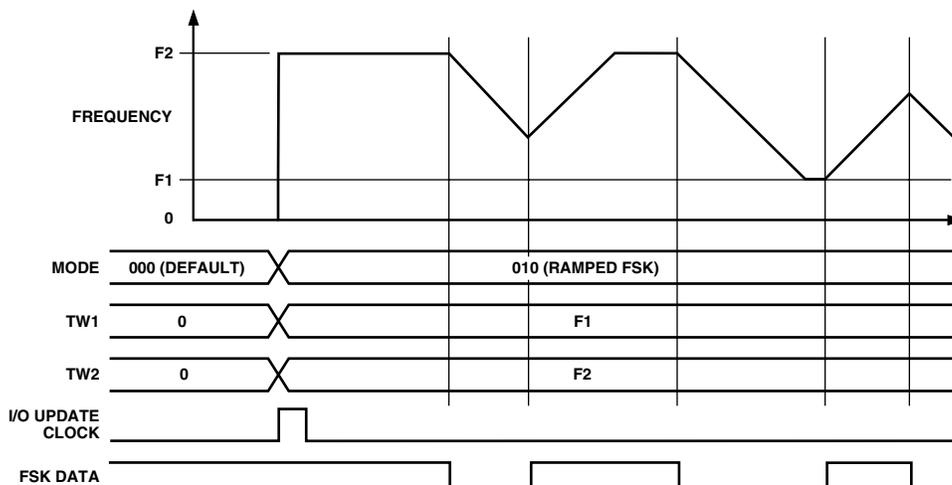


Figure 15. Effect of Premature Ramped FSK Data

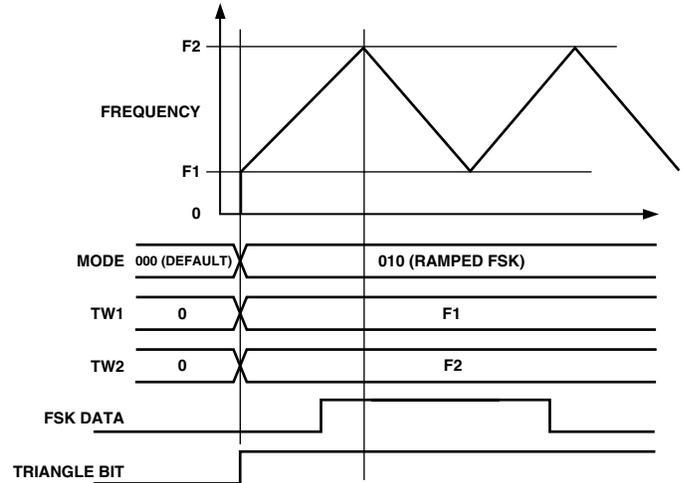


Figure 16. Automatic Linear Ramping Using the Triangle Bit

Additional flexibility in the ramped FSK mode is provided in the ability to respond to changes in the 48-bit delta frequency word and/or the 20-bit ramp-rate counter on-the-fly *during* the ramping from F1 to F2 or vice versa. To create these nonlinear frequency changes, it is necessary to combine several linear ramps, in a piecewise fashion, with differing slopes. This is done by programming and executing a linear ramp at some rate or "slope" and then altering the slope (by changing the ramp rate clock or delta frequency word or both). Changes in slope are made as often as needed to form the desired nonlinear frequency sweep response *before* the destination frequency has been reached. These piecewise changes can be precisely timed using the 32-bit Internal Update Clock (see detailed description of Update Clock in this data sheet).

Nonlinear ramped FSK will have the appearance of a chirp function that is graphically illustrated in Figure 17. The major difference between a ramped FSK function and a chirp function is that FSK is limited to operation between F1 and F2. Chirp operation has no F2 limit frequency.

Two additional control bits are available in the ramped FSK mode that allow even more options. CLR ACC1, register address 1F hex, will, if set high, clear the 48-bit *frequency accumulator* (ACC1) output with a retriggerable one-shot pulse of one system clock duration. If the CLR ACC1 bit is left high, a one-shot pulse will be delivered on the rising edge of every Update Clock. The effect is to interrupt the current ramp, reset the frequency back to the start point, F1 or F2, and then continue to ramp up (or down) at the previous rate. This will occur even when a static F1 or F2 destination frequency has been achieved.

Next, CLR ACC2 control bit (register address 1F hex) is available to clear both the *frequency accumulator* (ACC1) and the *phase accumulator* (ACC2). When this bit is set high, the output of the phase accumulator will result in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators will be cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low.

Chirp (Mode 011)

This mode is also known as pulsed FM. Most chirp systems use a linear FM sweep pattern, but the AD9852 supports nonlinear patterns, as well. In radar applications, use of chirp or pulsed FM allows operators to significantly reduce the output power needed to achieve the same result as a single-frequency radar system would produce. Figure 17 represents a very low resolution nonlinear chirp meant to demonstrate the different “slopes” that are created by varying the time steps (ramp rate) and frequency steps (delta frequency word).

The AD9852 permits precise, internally generated linear or externally programmed nonlinear pulsed or continuous FM over the complete frequency range, duration, frequency resolution and sweep direction(s). These are all user programmable. A block diagram of the FM chirp components is shown in Figure 18.

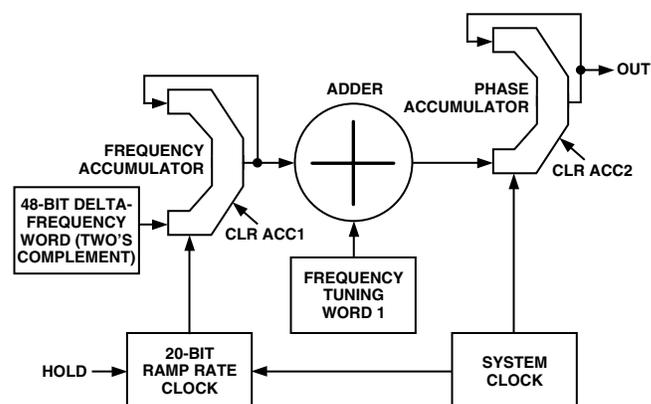


Figure 18. FM Chirp Components

Basic FM Chirp Programming Steps

1. Program a start frequency into Frequency Tuning Word 1 (parallel register addresses 4–9 hex) hereafter called FTW1.
2. Program the frequency step resolution into the 48-bit, *two's complement*, Delta Frequency Word (parallel register addresses 10–15 hex).
3. Program the rate of change (time at each frequency) into the 20-bit Ramp Rate Clock (parallel register addresses 1A–1C hex).
4. When programming is complete, an I/O update pulse at Pin 20 will engage the program commands.

The necessity for a two's complement Delta Frequency Word is to define the direction in which the FM chirp will move. If the 48-bit delta frequency word is negative (MSB is high) then the incremental frequency changes will be in a negative direction from FTW1. If the 48-bit word is positive (MSB is low), then the incremental frequency changes will be in a positive direction.

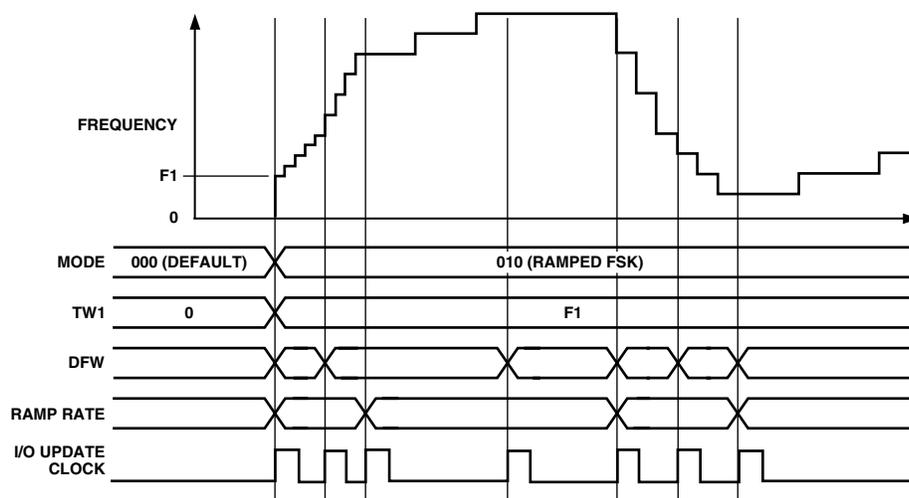


Figure 17. Example of a Nonlinear Chirp

AD9852

It is important to note that FTW1 is only a starting point for FM chirp. There is no built-in restraint requiring a return to FTW1. Once the FM chirp has begun, it is free to move (under program control) within the Nyquist bandwidth (dc to 1/2 system clock). *Instant* return to FTW1 is easily achieved, though, and this option is explained in the next few paragraphs.

Two control bits are available in the FM Chirp mode that will allow the return to the beginning frequency, FTW1, or to 0 Hz. First, when the CLR ACC1 bit (register address 1F hex) is set high, the 48-bit *frequency accumulator (ACC1) output* is cleared with a retriggerable one-shot pulse of one system clock duration. The 48-bit Delta Frequency Word input to the accumulator is unaffected by CLR ACC1 bit. If the CLR ACC1 bit is held high, a one-shot pulse will be delivered to the Frequency Accumulator (ACC1) on every rising edge of the I/O Update Clock. The effect is to interrupt the current chirp, reset the frequency back to FTW1, and continue the chirp at the previously programmed rate and direction. Clearing the output of the Frequency Accumulator in the chirp mode is illustrated in Figure 19. Shown in the diagram is the I/O Update Clock, which is either user-supplied or internally generated. A discussion of I/O Update is presented elsewhere in this data sheet.

Next, CLR ACC2 control bit (register address 1F hex) is available to clear both the *frequency accumulator (ACC1)* and the *phase accumulator (ACC2)*. When this bit is set high, the output of the phase accumulator will result in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators will be cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low. This bit is useful in generating pulsed FM.

Figure 20 graphically illustrates the effect of CLR ACC2 bit upon the DDS output frequency. Note that reprogramming the registers while the CLR ACC2 bit is high allows a new FTW1 frequency and slope to be loaded.

Another function available only in the chirp mode is the HOLD pin, Pin 29. This function will stop the clock signal to the ramp rate counter, thereby halting any further clocking pulses to the frequency accumulator, ACC1. The effect is to halt the chirp

at the frequency existing just before HOLD was pulled high. When the HOLD pin is returned low, the clocks are resumed and chirp continues. During a hold condition, the user may change the programming registers; however, the ramp rate counter must resume operation at its previous rate until a count of zero is obtained before a new ramp rate count can be loaded. Figure 21 illustrates the effect of the hold function on the DDS output frequency.

The 32-bit automatic I/O Update counter may be used to construct complex chirp or ramped FSK sequences. Since this internal counter is synchronized with the AD9852 System Clock, it allows precisely timed program changes to be invoked. In this manner, the user is only required to reprogram the desired registers before the automatic I/O Update Clock is generated.

In the chirp mode, the destination frequency is not directly specified. If the user fails to control the chirp, the DDS will naturally confine itself to the frequency range between dc and Nyquist. Unless terminated by the user, the chirp will continue until power is removed.

When the chirp destination frequency is reached there are several possible outcomes:

1. Stop at the destination frequency using the HOLD pin, or by loading all zeros into the Delta Frequency Word registers of the frequency accumulator (ACC1).
2. Use the HOLD pin function to stop the chirp, then ramp-down the output amplitude using the digital multiplier stages and the Shaped Keying pin, Pin 30, or via program register control (addresses 21–24 hex).
3. Abruptly terminate the transmission using the CLR ACC2 bit.
4. Continue chirp by reversing direction and returning to the previous, or another, destination frequency in a linear or user-directed manner. If this involves going down in frequency, a negative 48-bit Delta Frequency Word (the MSB is set to “1”) must be loaded into registers 10–15 hex. Any decreasing frequency step of the Delta Frequency Word requires the MSB to be set to logic high.

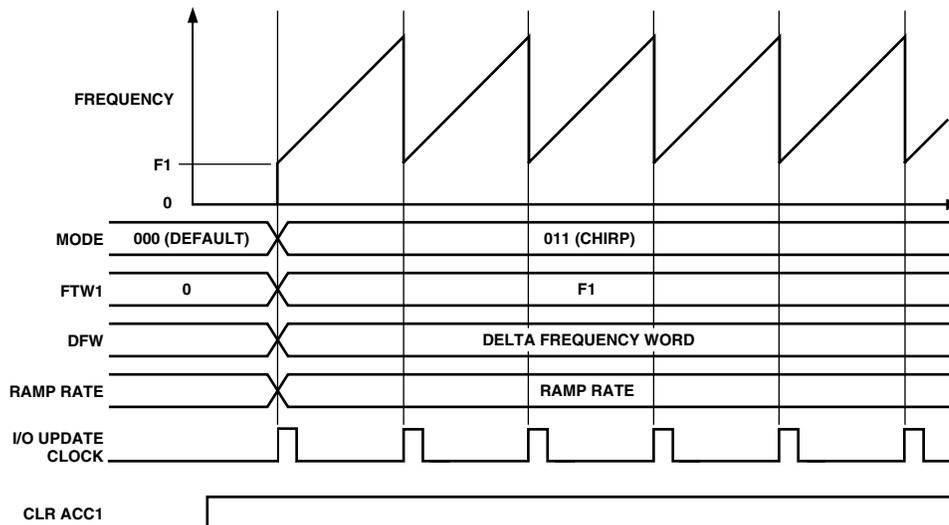


Figure 19. Effect of CLR ACC1 in FM Chirp Mode

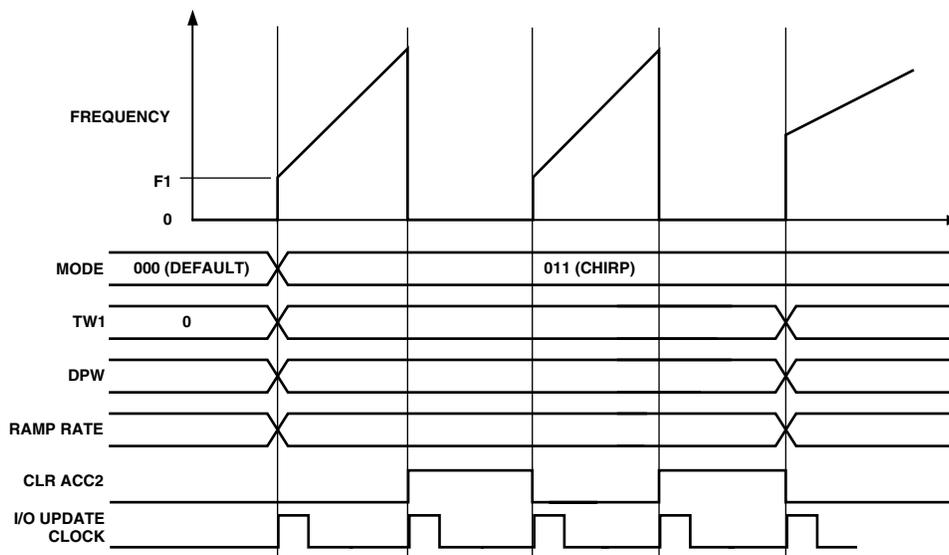


Figure 20. Effect of CLR ACC2 in FM Chirp Mode

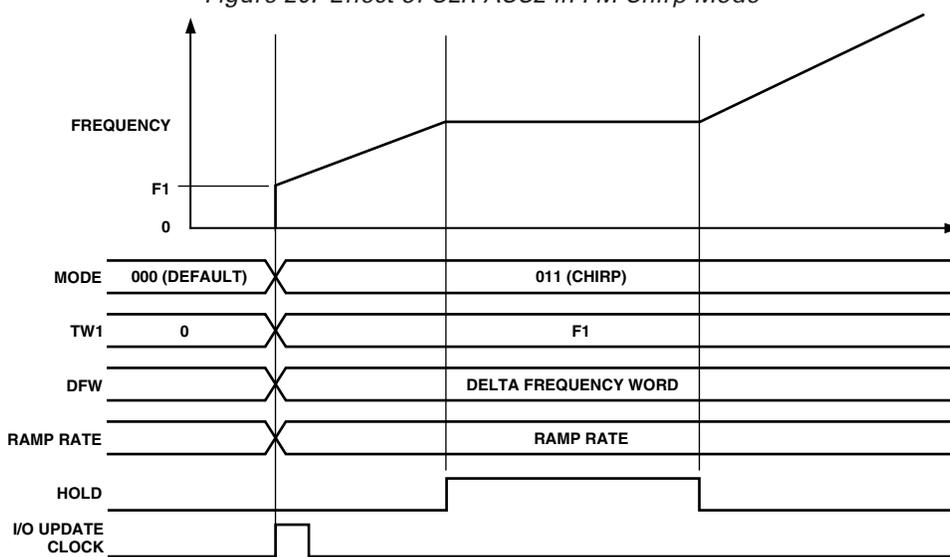


Figure 21. Illustration of HOLD Function

- Continue chirp by immediately returning to the beginning frequency (F1) in a sawtooth fashion and repeat the previous chirp process. This is where CLR ACC1 control bit is used. An automatic, repeating chirp can be set up using the 32-bit Update Clock to issue CLR ACC1 command at precise time intervals. Adjusting the timing intervals or changing the Delta Frequency Word will change the chirp range. It is incumbent upon the user to balance the chirp duration and frequency resolution to achieve the proper frequency range.

BPSK (Mode 100)

Binary, biphasic or bipolar phase shift keying is a means to rapidly select between two preprogrammed 14-bit output phase offsets. The logic state of Pin 29, BPSK pin, controls the selection of Phase Adjust Register number 1 or 2. When low, Pin 29 selects Phase Adjust Register 1; when high, Phase Adjust Register 2 is selected. Figure 22 illustrates phase changes made to four cycles of an output carrier.

Basic BPSK programming steps:

- Program a carrier frequency into Frequency Tuning Word 1.
- Program appropriate 14-bit phase words in Phase Adjust Registers 1 and 2.
- Attach BPSK data source to Pin 29.
- Activate I/O Update Clock when ready.

NOTE: If higher order PSK modulation is desired, the user should select the Single-Tone mode and program Phase Adjust Register 1 using the serial or high-speed parallel programming bus.

USING THE AD9852

Internal and External Update Clock

This function is comprised of a bidirectional I/O pin, Pin 20, and a programmable 32-bit down-counter. In order for programming changes to be transferred from the I/O Buffer registers to the active core of the DDS, a clock signal (low to high edge) must be externally supplied to Pin 20 or internally generated by the 32-bit Update Clock.

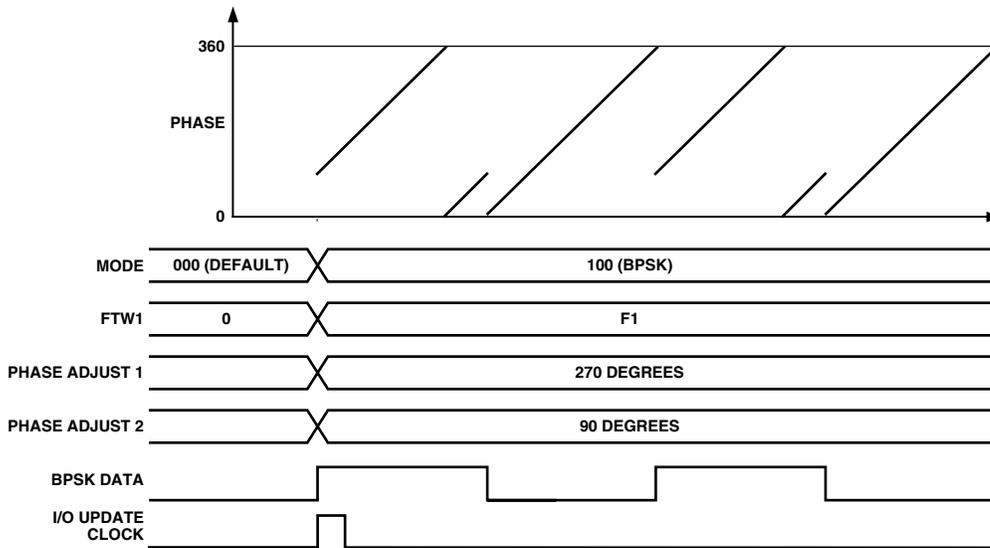


Figure 22. BPSK Mode

When the user provides an external Update Clock, it is internally synchronized with the system clock to prevent partial transfer of program register information due to violation of data setup or hold times. This mode gives the user complete control of when updated program information becomes effective. The default mode for Update Clock is internal (Int Update Clk control register bit is logic high). To switch to External Update Clock mode, the Int Update Clk register bit must be set to logic low. The internal update mode generates automatic, periodic update pulses with the time period set by the user.

An internally generated Update Clock can be established by programming the 32-bit Update Clock registers (address 16–19 hex) and setting the Int Update Clk (address 1F hex) control register bit to logic high. The update clock down-counter function operates at 1/2 the rate of the system clock (150 MHz maximum) and counts down from a 32-bit binary value (programmed by the user). When the count reaches 0, an automatic I/O Update of the DDS output or functions is generated. The update clock is internally and externally routed on Pin 20 to allow users to synchronize programming of update information with the update clock rate. The time period between update pulses is given as:

$$(N + 1) \times \text{SYSTEM CLOCK PERIOD}$$

where N is the 32-bit value programmed by the user. Allowable range of N is from 1 to $(2^{32} - 1)$. The internally generated update pulse output on Pin 20 has a fixed high time of eight system clock cycles.

Programming the Update Clock register for values less than five will cause the I/O UD pin to remain high. The update clock functionality still works; however, the user cannot use the signal as an indication that data is transferring. This is an effect of the minimum high pulse time when I/O UD is an output.

Shaped On/Off Keying

This feature allows the user to control the amplitude vs. time slope of the cosine DAC output signal. This function is used in “burst transmissions” of digital data to reduce the adverse spectral impact of short, abrupt bursts of data. Users must first enable the digital multiplier by setting the OSK EN bit (control register address 20 hex) to logic high in the control register.

Otherwise, if the OSK EN bit is set low, the digital multiplier responsible for amplitude control is bypassed and the cosine DAC output is set to full-scale amplitude. In addition to setting the OSK EN bit, a second control bit, OSK INT (also at address 20 hex), must be set to logic high. Logic high selects the linear internal control of the output ramp-up or ramp-down function. A logic low in the OSK INT bit switches control of the digital multiplier to user programmable 12-bit register allowing users to dynamically shape the amplitude transition in practically any fashion. The 12-bit register, labeled “Output Shape Key,” is located at addresses 21–22 hex in Table IV. The maximum output amplitude is a function of the R_{SET} resistor and is not programmable when OSK INT is enabled.

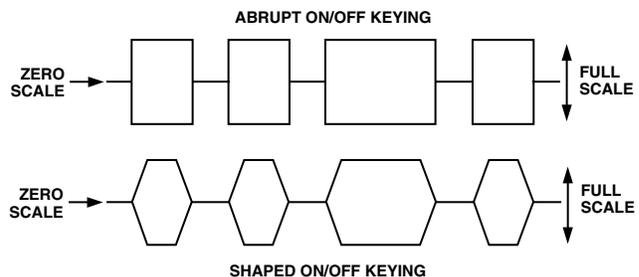


Figure 23. Shaped On/Off Keying

The transition time from zero-scale to full-scale must also be programmed. The transition time is a function of two fixed elements and one variable. The variable element is the programmable 8-bit RAMP RATE COUNTER. This is a down-counter that is clocked at the system clock rate (300 MHz max) and generates one pulse whenever the counter reaches zero. This pulse is routed to a 12-bit counter that increments with each pulse received. The outputs of the 12-bit counter are connected to the 12-bit digital multiplier. When the digital multiplier has a value of all zeros at its inputs, the input signal is multiplied by zero, producing zero-scale. When the multiplier has a value of all ones, the input signal is multiplied by a value of 4095/4096, producing nearly full-scale. There are 4094 remaining fractional multiplier values that will produce output amplitudes scaled according to their binary values.

AD9852

Inverse SINC Function

This filter precompensates input data to the cosine DAC for the $\text{SIN}(x)/x$ roll-off characteristic inherent in the DAC's output spectrum. This allows wide bandwidth signals (such as QPSK) to be output from the DAC without appreciable amplitude variations as a function of frequency. The inverse SINC function may be bypassed to *significantly* reduce power consumption, especially at higher clock speeds.

Inverse SINC is engaged by default and is bypassed by bringing the "Bypass Inv SINC" bit high in control register 20 (hex) in Table IV.

REFCLK Multiplier

This is a programmable PLL-based reference clock multiplier that allows the user to select an integer clock multiplying value over the range of $4\times$ to $20\times$. Use of this function allows users to input as little as 15 MHz at the REFCLK input to produce a 300 MHz internal system clock. Five bits in control register 1E hex set the multiplier value as follows in Table III.

The REFCLK Multiplier function can be bypassed to allow direct clocking of the AD9852 from an external clock source. The system clock for the AD9852 is either the output of the REFCLK Multiplier (if it is engaged) or the REFCLK inputs. REFCLK may be either a single-ended or differential input by setting Pin 64, DIFF CLK ENABLE, low or high respectively.

PLL Range Bit

The PLL Range Bit selects the frequency range of the REFCLK Multiplier PLL. For operation from 200 MHz to 300 MHz (internal system clock rate) the PLL Range Bit should be set to Logic 1. For operation below 200 MHz, the PLL Range Bit should be set to Logic 0. The PLL Range Bit adjusts the PLL loop parameters for optimized phase noise performance within each range.

Pin 61, PLL FILTER

This pin provides the connection for the external zero compensation network of the PLL loop filter. The zero compensation network consists of a 1.3 k Ω resistor in series with a 0.01 μF capacitor. The other side of the network should be connected as close as possible to Pin 60, AVDD. For optimum phase noise performance, the clock multiplier can be bypassed by setting the "Bypass PLL" bit in control register address 1E.

Differential REFCLK Enable

A high level on this pin enables the differential clock inputs, REFCLK and REFCLKB (Pins 69 and 68 respectively). The minimum differential signal amplitude required is 400 mV p-p at the REFCLK input pins. The centerpoint or common-mode range of the differential signal can range from 1.6 V to 1.9 V.

When Pin 64 (DIFF CLK ENABLE) is tied low, REFCLK (Pin 69) is the only active clock input. This is referred to as the *single-ended* mode. In this mode, Pin 68 (REFCLKB) should be tied low or high.

High-Speed Comparator—Optimized for high speed, >300 MHz toggle rate, low jitter, sensitive input, built-in hysteresis and an output level of 1 V p-p minimum into 50 Ω or CMOS logic levels into high impedance loads. The comparator can be separately powered down to conserve power. This comparator is used in "clock generator" applications to square up the filtered sine wave generated by the DDS.

Power-Down—Several individual stages may be powered down to reduce power consumption via the programming registers while still maintaining functionality of desired stages. These stages are identified in the Register Layout table, address 1D hex. Power-down is achieved by setting the specified bits to logic high. A logic low indicates that the stages are powered up.

Furthermore, and perhaps most significantly, the Inverse Sinc filters and the Digital Multiplier stages, can be bypassed to achieve significant power reduction through programming of the control registers in address 20 hex. Again, logic high will cause the stage to be bypassed. Of particular importance is the Inverse Sinc filter as this stage consumes a significant amount of power.

A full power-down occurs when all four PD bits in control register 1D hex are set to logic high. This reduces power consumption to approximately 10 mW (3 mA).

PROGRAMMING THE AD9852

The AD9852 Register Layout, shown in Table IV, contains the information that programs the chip for the desired functionality. While many applications will require very little programming to configure the AD9852, some will make use of all twelve accessible register banks. The AD9852 supports an 8-bit parallel I/O operation or an SPI-compatible serial I/O operation. All accessible registers can be written and read back in either I/O operating mode.

S/P SELECT, Pin 70, is used to configure the I/O mode. Systems that use the parallel I/O mode must connect the S/P SELECT pin to V_{DD} . Systems that operate in the serial I/O mode must tie the S/P SELECT pin to GND.

Regardless of mode, the I/O port data is written to a buffer memory that does *not* affect operation of the part until the contents of the buffer memory are transferred to the register banks. This transfer of information occurs synchronously to the system clock and occurs in one of two ways:

1. Internally controlled at a rate programmable by the user, or
2. Externally controlled by the user. I/O operations can occur in the absence of REFCLK but the data cannot be moved from the buffer memory to the register bank without REFCLK. See the Update Clock Operation section of this document for details.

Master RESET—Logic high active, must be held high for a minimum of 10 system clock cycles. This causes the communications bus to be initialized and loads default values listed in Table IV.

Parallel I/O Operation

With the S/P SELECT pin tied high, the parallel I/O mode is active. The I/O port is compatible with industry standard DSPs and microcontrollers. Six address bits, eight bidirectional data bits and separate write/read control inputs make up the I/O port pins.

Parallel I/O operation allows write access to each byte of any register in a single I/O operation up to 1/10.5 ns. Read back capability for each register is included to ease designing with the AD9852.

Reads are not guaranteed at 100 MHz as they are intended for software debug only.

Parallel I/O operation timing diagrams are shown in Figures 26 and 27.

Table III. REFCLK Multiplier Control Register Values

Multiplier Value	Ref Mult Bit 4	Ref Mult Bit 3	Ref Mult Bit 2	Ref Mult Bit 1	Ref Mult Bit 0
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0

Serial Port I/O Operation

With the S/P SELECT pin tied low, the serial I/O mode is active. The AD9852 serial port is a flexible, synchronous, serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols. The interface allows read/write access to all twelve registers that configure the AD9852 and can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO). Data transfers are supported in most significant bit (MSB) first format or least significant bit (LSB) first format at up to 10 MHz.

When configured for serial I/O operation, most pins from the AD9852 parallel port are inactive; some are used for the serial I/O. Table V describes pin requirements for serial I/O.

Note: When operating in the serial I/O mode, it is best to use the external I/O update CLK mode to avoid an I/O update CLK during a serial communication cycle. Such an occurrence could cause incorrect programming due to partial data transfer. Hence, the user would want to write between I/O update CLKs. To exit the default internal update mode, at power-up, before starting the REFCLK signal, but after a Master Reset, program the device for external update operation. Starting the REFCLK will cause this information to transfer to the register bank, putting the device in external update mode.

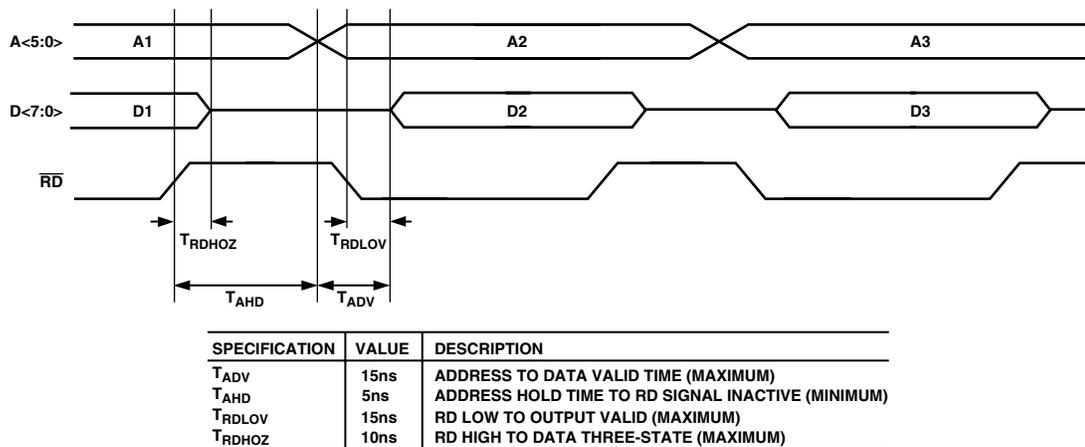


Figure 26. Parallel Port Read Timing Diagram

Table IV. Register Layout. Shaded Sections Comprise the Control Register

Parallel Address	Serial Address	AD9852 Register Layout								Default Value
Hex	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
00 01	0	Phase Adjust Register #1 <13:8> (Bits 15, 14 don't care)				Phase 1				00h 00h
02 03	1	Phase Adjust Register #2 <13:8> (Bits 15, 14 don't care)				Phase 2				00h 00h
04 05 06 07 08 09	2	Frequency Tuning Word 1 <47:40>				Frequency 1				00h 00h 00h 00h 00h 00h
0A 0B 0C 0D 0E 0F	3	Frequency Tuning Word 2 <47:40>				Frequency 2				00h 00h 00h 00h 00h 00h
10 11 12 13 14 15	4	Delta Frequency Word <47:40>								00h 00h 00h 00h 00h 00h
16 17 18 19	5	Update Clock <31:24>								00h 00h 00h 40h
1A 1B 1C	6	Ramp Rate Clock <19:16> (Bits 23, 22, 21, 20 don't care)								00h 00h 00h
1D	7	Don't Care	Don't Care	Don't Care	Comp PD	Reserved, Always Low	Control DAC PD	DAC PD	DIG PD	10h
1E		Don't Care	PLL Range	Bypass PLL	Ref Mult 4	Ref Mult 3	Ref Mult 2	Ref Mult 1	Ref Mult 0	64h
1F		CLR ACC 1	CLR ACC 2	Triangle	Don't Care	Mode 2	Mode 1	Mode 0	INT/EXT Update Clk	01h
20		Don't Care	Bypass Inv Sinc	OSK EN	OSK INT	Don't Care	Don't Care	LSB First	SDO Active CR [0]	20h
21 22	8	Output Shape Key Mult <11:8> (Bits 15, 14, 13, 12 don't care)								00h 00h
23 24	9	Don't Care								00h 00h
25	A	Output Shape Key Ramp Rate <7:0>								80h
26 27	B	Control DAC <11:8> (Bits 15, 14, 13, 12 don't care)								00h 00h
		Control DAC <7:0> (Data is required to be in two's complement format)								00h

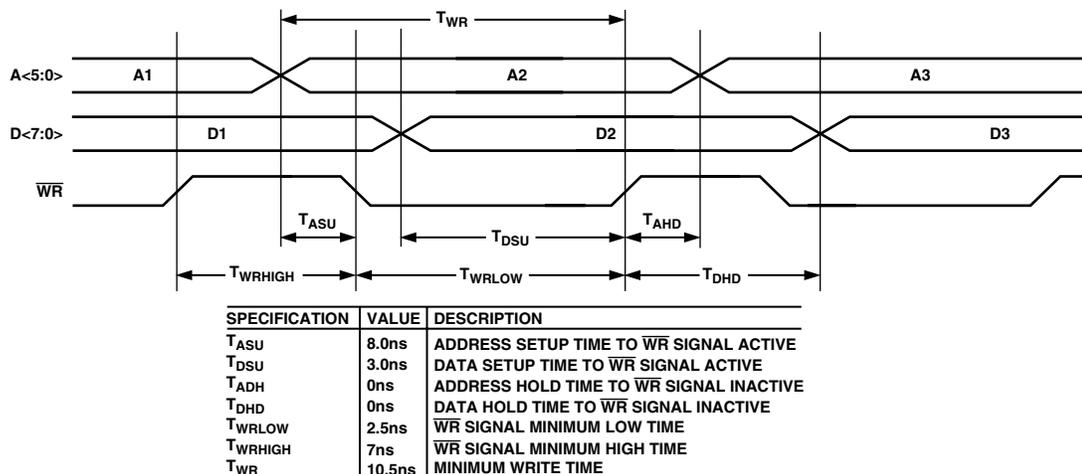


Figure 27. Parallel Port Write Timing Diagram

Table V. Serial I/O Pin Requirements

Pin Number	Pin Name	Serial I/O Description
1, 2, 3, 4, 5, 6, 7, 8	D[7:0]	The parallel data pins are not active, tie to VDD or GND.
14, 15, 16	A[5:3]	The parallel address Pins A5, A4, A3 are not active, tie to VDD or GND.
17	A2	I/O RESET
18	A1	SDO
19	A0	SDIO
20	I/O UD CLOCK	Update Clock. Same functionality for Serial Mode as Parallel Mode.
21	WRB	SCLK
22	RDB	CSB—Chip Select

Table VI. Register Address vs. Data Bytes Transferred

Serial Register Address	Register Name	Number of Bytes Transferred
0	Phase Offset Tuning Word Register #1	2 Bytes
1	Phase Offset Tuning Word Register #2	2 Bytes
2	Frequency Tuning Word #1	6 Bytes
3	Frequency Tuning Word #2	6 Bytes
4	Delta Frequency Register	6 Bytes
5	Update Clock Rate Register	4 Bytes
6	Ramp Rate Clock Register	3 Bytes
7	Control Register	4 Bytes
8	Digital Multiplier Register	2 Bytes
A	Shaped On/Off Keying Ramp Rate Register	1 Byte
B	Control DAC Register	2 Bytes

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a serial communication cycle with the AD9852. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9852, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9852 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, and the register address to be acted upon.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9852. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9852 and the system controller. The number of data bytes transferred in Phase 2 of the communication cycle is a function of the register address. The AD9852 internal serial I/O controller expects every byte of the register being accessed to be transferred. Table VI describes how many bytes must be transferred.

At the completion of any communication cycle, the AD9852 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle. In addition, an active high input on the I/O RESET pin immediately terminates the current communication cycle. After I/O RESET returns low, the AD9852 serial port controller requires the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9852 is registered on the rising edge of SCLK. All data is driven out of the AD9852 on the falling edge of SCLK.

Figures 28 and 29 are useful in understanding the general operation of the AD9852 Serial Port.

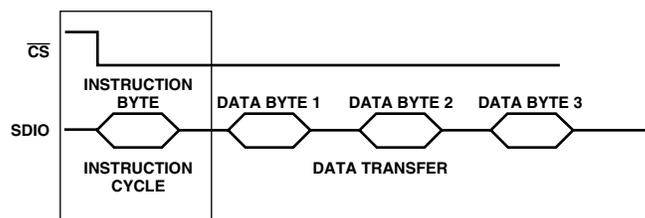


Figure 28. Using SDIO as a Read/Write Transfer

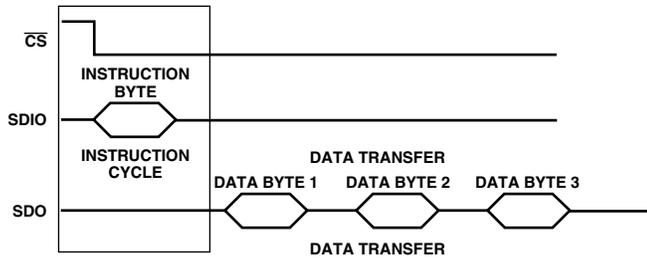


Figure 29. Using SDIO as an Input, SDO as an Output

Instruction Byte

The instruction byte contains the following information.

Table VII. Instruction Byte Information

MSB	D6	D5	D4	D3	D2	D1	LSB
R/W	X	X	X	A3	A2	A1	A0

R/W—Bit 7 of the instruction byte determines whether a read or write data transfer will occur following the instruction byte. Logic high indicates read operation. Logic zero indicates a write operation.

Bits 6, 5, and 4 of the instruction byte are dummy bits (don't care).

A3, A2, A1, A0—Bits 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. See Table VI for register address details.

Serial Interface Port Pin Description

SCLK

Serial Clock (Pin 21). The serial clock pin is used to synchronize data to and from the AD9852 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

CS

Chip Select (Pin 22). Active low input that allows more than one device on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until CS is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO

Serial Data I/O (Pin 19). Data is always written into the AD9852 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 0 of register address 20h. The default is logic zero, which configures the SDIO pin as bidirectional.

SDO

Serial Data Out (Pin 18). Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9852 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

I/O RESET

Synchronize I/O Port (Pin 17). Synchronizes the I/O port state machines without affecting the contents of the addressable registers. An active high input on I/O RESET pin causes the current communication cycle to terminate. After I/O RESET returns low (Logic 0) another communication cycle may begin, starting with the instruction byte.

Notes on Serial Port Operation

The AD9852 serial port configuration bits reside in Bits 1 and 0 of register address 20h. It is important to note that the configuration changes *immediately* upon a valid I/O update. For multibyte transfers, writing this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.

The system must maintain synchronization with the AD9852 or the internal control logic will not be able to recognize further instructions. For example, if the system sends the instruction to write a 2-byte register, then pulses the SCLK pin for a 3-byte register (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9852, but the next eight rising SCLK edges are interpreted as the next instruction byte, *not* the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9852, the I/O RESET pin provides a means to reestablish synchronization without reinitializing the entire chip. Asserting the I/O RESET pin (active high) resets the AD9852 serial port state machine, terminating the current I/O operation and putting the device into a state in which the next eight SCLK rising edges are understood to be an instruction byte. The I/O RESET pin must be deasserted (low) before the next instruction byte write can begin. Any information that had been written to the AD9852 registers during a valid communication cycle prior to loss of synchronization will remain intact.

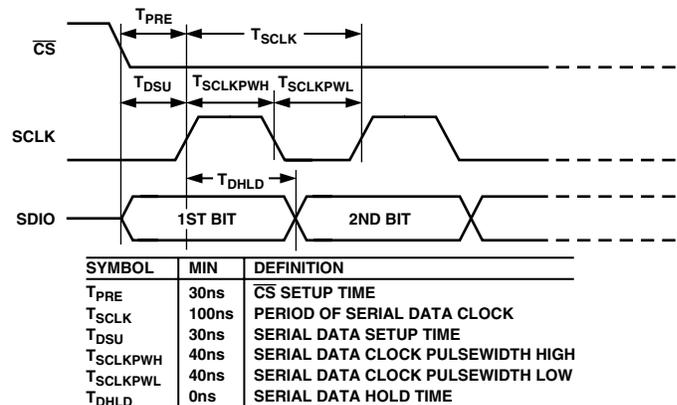


Figure 30. Timing Diagram for Data Write to AD9852

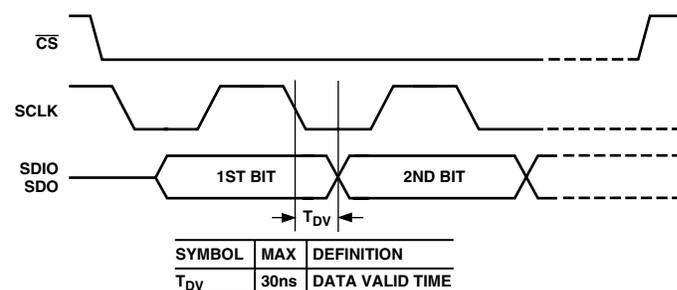


Figure 31. Timing Diagram for Read from AD9852

MSB/LSB TRANSFERS

The AD9852 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by Bit 1 of serial register bank 20h. When this bit is set active high, the AD9852 serial port is in LSB first format. This bit defaults low, to the MSB first format. The instruction byte must be written in the format indicated by Bit 1 of serial register bank 20h. That is, if the AD9852 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

Control Register Description

The Control Register is located in the shaded portion of Table IV at address 1D through 20 hex. It is composed of 32 bits. Bit 31 is located at the top left position and Bit 0 is located in the lower right position of the shaded table portion. The register has been subdivided below to make it easier to locate the text associated with specific control categories.

CR[31:29] are open.

CR[28] is the comparator power-down bit. When set (Logic 1), this signal indicates to the comparator that a power-down mode is active. This bit is an output of the digital section and is an input to the analog section.

CR[27] must always be written to logic zero. Writing this bit to Logic 1 causes the AD9852 to stop working until a master reset is applied.

CR[26] is the control DAC power-down bit. When set (Logic 1), this signal indicates to the control DAC that a power-down mode is active.

CR[25] is the full DAC power-down bit. When set (Logic 1), this signal indicates to both the cosine and control DACs as well as the reference that a power-down mode is active.

CR[24] is the digital power-down bit. When set (Logic 1), this signal indicates to the digital section that a power-down mode is active. Within the digital section, the clocks will be forced to dc, effectively powering down the digital section. The PLL will still accept the REFCLK signal and continue to output the higher frequency.

CR[23] is reserved. Write to zero.

CR[22] is the PLL range bit. The PLL range bit controls the VCO gain. The power-up state of the PLL range bit is Logic 1, higher gain for frequencies above 200 MHz.

CR[21] is the bypass PLL bit, active high. When active, the PLL is powered down and the REFCLK input is used to drive the system clock signal. The power-up state of the bypass PLL bit is Logic 1, PLL bypassed.

CR[20:16] bits are the PLL multiplier factor. These bits are the REFCLK multiplication factor unless the bypass PLL bit is set. The PLL multiplier valid range is from 4 to 20, inclusive.

CR[15] is the clear accumulator 1 bit. This bit has a one-shot type function. When written active, Logic 1, a clear accumulator 1 signal is sent to the DDS logic, resetting the accumulator value to zero. The bit is then automatically reset, but the buffer memory is not reset. This bit allows the user to easily create a sawtooth frequency sweep pattern with minimal user intervention. This bit is intended for chirp mode only, but its function is still retained in other modes.

CR[14] is the clear accumulator bit. This bit, active high, holds both the accumulator 1 and accumulator 2 values at zero for as long as the bit is active. This allows the DDS phase to be initialized via the I/O port.

CR[13] is the triangle bit. When this bit is set, the AD9852 will automatically perform a continuous frequency sweep from F1 to F2 frequencies and back. The effect is a triangular frequency sweep. When this bit is set, the operating mode must be set to ramped FSK.

CR[12] Don't Care.

CR[11:9] are the three bits that describe the five operating modes of the AD9852:

0h = Single-Tone Mode

1h = FSK Mode

2h = Ramped FSK mode

3h = Chirp Mode

4h = BPSK Mode

CR[8] is the internal update active bit. When this bit is set to Logic 1, the I/O UD pin is an output and the AD9852 generates the I/O UD signal. When Logic 0, external I/O UD functionality is performed, the I/O UD pin is configured as an input.

CR[7] is reserved. Write to zero.

CR[6] is the inverse sinc filter BYPASS bit. When set, the data from the DDS block goes directly to the output shaped-keying logic and the clock to the inverse sinc filter is stopped. Default is clear, filter enabled.

CR[5] is the shaped-keying enable bit. When set, the output ramping function is enabled and is performed in accordance with the CR[4] bit requirements.

CR[4] is the internal/external output shaped-keying control bit. When set to Logic 1, the shaped-keying factor will be internally generated and applied to the cosine DAC path. When cleared (default), the output shaped-keying function is externally controlled by the user and the shaped-keying factor is the shaped-keying factor register's value. The two registers that are the shaped-keying factors also default low such that the output is off at power-up and until the device is programmed by the user.

CR[3:2] are reserved. Write to zero.

CR[1] is the serial port MSB/LSB first bit. Defaults low, MSB first.

CR[0] is the serial port SDO active bit. Defaults low, inactive.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9852 is a multifunctional, very high-speed device that targets a wide variety of synthesizer and agile clock applications. The set of numerous innovative features contained in the device each consume incremental power. If enabled in combination, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management is a critical element in the successful application of the AD9852 device.

The AD9852 device is specified to operate within the industrial temperature range of -40°C to $+85^{\circ}\text{C}$. This specification is conditional, however, such that the absolute maximum junction temperature of 150°C is not exceeded. At high operating temperatures, extreme care must be taken in the operation of the device

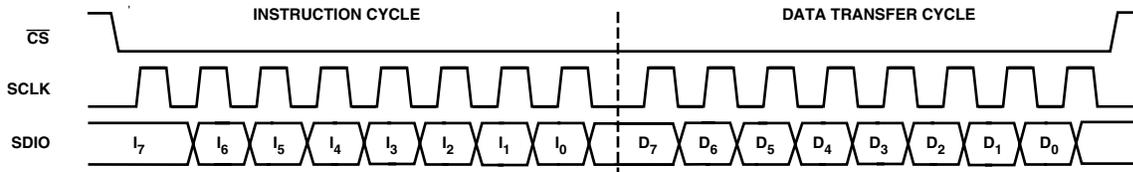


Figure 32. Serial Port Write Timing—Clock Stall Low

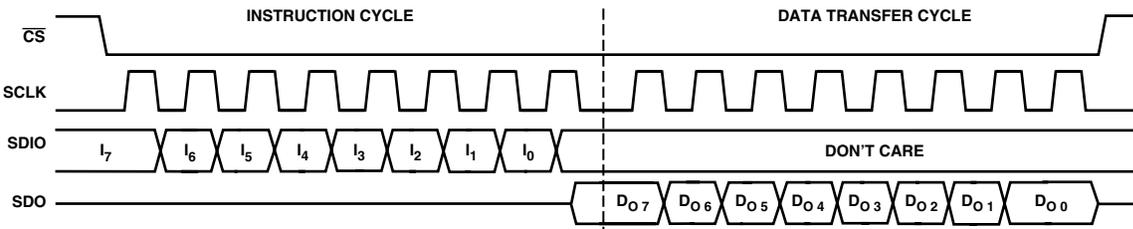


Figure 33. Three-Wire Serial Port Read Timing—Clock Stall Low

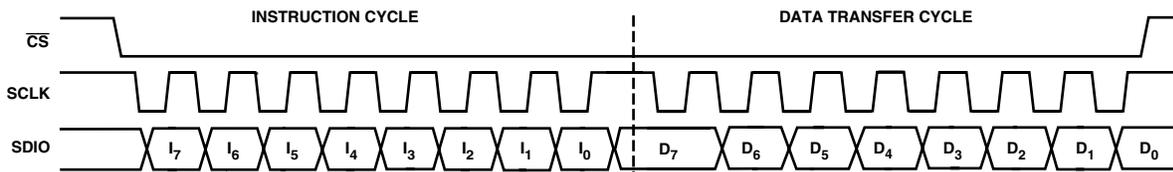


Figure 34. Serial Port Write Timing—Clock Stall High

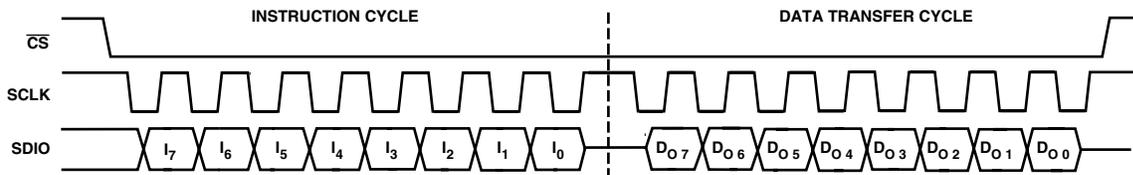


Figure 35. Two-Wire Serial Port Read Timing—Clock Stall High

to avoid exceeding the junction temperature which results in a potentially damaging thermal condition.

Many variables contribute to the operating junction temperature within the device, including:

1. Package Style
2. Selected Mode of Operation
3. Internal System Clock Speed
4. Supply Voltage
5. Ambient Temperature.

The combination of these variables determines the junction temperature within the AD9852 device for a given set of operating conditions.

The AD9852 device is available in two package styles: a thermally enhanced surface-mount package with an exposed heat sink, and a nonthermally enhanced surface-mount package. The thermal impedance of these packages is 16°C/W and 38°C/W respectively, measured under still-air conditions.

THERMAL IMPEDANCE

The thermal impedance of a package can be thought of as a thermal resistor that exists between the semiconductor surface and the ambient air. The thermal impedance of a package is determined by package material and its physical dimensions. The dissipation of the heat from the package is directly dependent upon the ambient air conditions and the physical connection made between the IC package and the PCB. Adequate dissipation of power from the AD9852 relies upon all power and ground pins of the device being soldered directly to a copper plane on a PCB. In addition, the thermally enhanced package of the AD9852ASQ contains a heat sink on the bottom of the package that must be soldered to a ground pad on the PCB surface. This pad must be connected to a large copper plane which, for convenience, may be ground plane. Sockets for either package style of the AD9852 device are not recommended.

JUNCTION TEMPERATURE CONSIDERATIONS

The power dissipation (P_{DISS}) of the AD9852 device in a given application is determined by many operating conditions. Some of the conditions have a direct relationship with P_{DISS} , such as supply voltage and clock speed, but others are less deterministic. The total power dissipation within the device, and its effect on the junction temperature, must be considered when using the device. The junction temperature of the device is given by:

$$\text{Junction Temperature} = (\text{Thermal Impedance} \times \text{Power Consumption}) + \text{Ambient Temperature}$$

Given that the junction temperature should never exceed 150°C for the AD9852, and that the ambient temperature can be 85°C, the maximum power consumption for the AD9852AST is 1.7 W and the AD9852ASQ (thermally enhanced package) is 4.1 W. Factors affecting the power dissipation are:

Supply Voltage—This obviously affects power dissipation and junction temperature since P_{DISS} equals $V \times I$. Users should design for 3.3 V nominal; however, the device is guaranteed to meet specifications, over the full temperature range and over the supply voltage range of 3.135 V to 3.465 V.

Clock Speed—This directly and linearly influences the total power dissipation of the device, and, therefore, junction temperature. As a rule, the user should always select the lowest internal clock speed possible to support a given application, to minimize power dissipation. Normally the usable frequency output bandwidth from a DDS is limited to 40% of the clock rate to keep reasonable requirements on the output low-pass filter. For the typical DDS application, the system clock frequency should be 2.5 times the highest desired output frequency.

Mode of Operation—The selected mode of operation for the AD9852 has a great influence on total power consumption. The AD9852 offers many features and modes, each of which imposes an additional power requirement. The collection of features contained in the AD9852 targets a wide variety of applications and the device was designed under the assumption that only a few features would be enabled for any given application. In fact, the user must understand that enabling multiple features at higher clock speeds may cause the maximum junction temperature of the die to be exceeded. This can severely limit the long-term reliability of the device. Figures 36a and 36b provide a summary of the power requirements associated with the individual features of the AD9852. These charts should be used as a guide in determining the optimum application of the AD9852 for reliable operation.

As can be seen in Figure 36b, the Inverse Sinc filter function requires a significant amount of power. As an alternate approach to maintaining flatness across the output bandwidth, the digital multiplier function may be used to adjust the output signal level, at a dramatic savings in power consumption. Careful planning and management in the use of the feature set will minimize power dissipation and avoid exceeding junction temperature requirements within the IC.

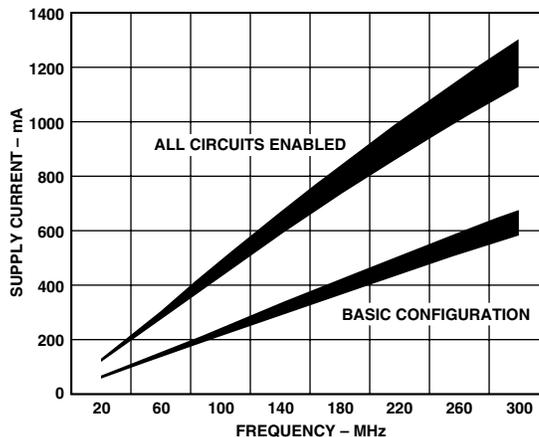


Figure 36a. Current Consumption vs. Clock Frequency

Figure 36a shows the supply current consumed by the AD9852 over a range of frequencies for two possible configurations: *all circuits enabled* means the output scaling multiplier, the inverse sinc filter, both DACs, and the on-board comparator are all enabled. *Basic configuration* means the output scaling multipliers, the inverse sinc filter, the control DAC, and the on-board comparator are all disabled.

Figure 36b shows the approximate current consumed by each of four functions.

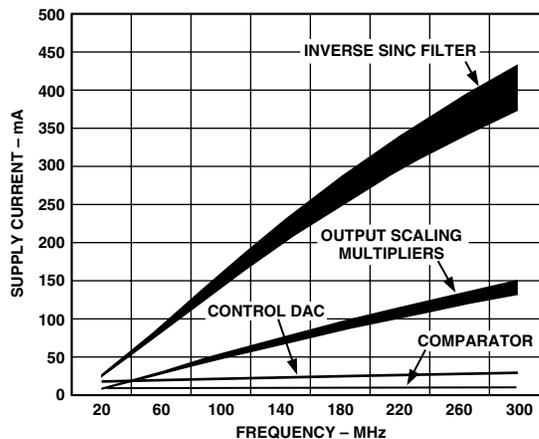


Figure 36b. Current Consumption by Function vs. Clock Frequency

EVALUATION OF OPERATING CONDITIONS

The first step in applying the AD9852 is to select the internal clock frequency. Clock frequency selections above 200 MHz will require the thermally enhanced package (AD9852ASQ); clock frequency selections of 200 MHz and below may allow the use of the standard plastic surface-mount package, but more information will be needed to make that determination.

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The second step is to determine the maximum required operating temperature for the AD9852 in the given application. Subtract this value from 150°C, which is the maximum junction temperature allowed for the AD9852. For the extended industrial temperature range, the maximum operating temperature is 85°C, which results in a difference of 65°C. This is the maximum temperature gradient that the device may experience due to power dissipation.

The third step is to divide this maximum temperature gradient by the thermal impedance, to arrive at the maximum power dissipation allowed for the application. For the example so far, 65°C divided by both versions of the AD9852 package's thermal impedances of 38°C/W and 16°C/W, yields a total power dissipation limit of 1.7 W and 4.1 W (respectively). This means that for a 3.3 V nominal power supply voltage, the current consumed by the device under full operating conditions must not exceed 515 mA in the standard plastic package and 1242 mA in the thermally enhanced package. The total set of enabled functions and operating conditions of the AD9852 application must support these current consumption limits.

Figures 36a and 36b may be used to determine the suitability of a given AD9852 application vs. power dissipation requirements. These graphs assume that the AD9852 device will be soldered to a multilayer PCB per the recommended best manufacturing practices and procedures for the given package type. This ensures that the specified thermal impedance specifications will be achieved.

THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES

The following are general recommendations for mounting the thermally enhanced exposed heat sink package (AD9852ASQ) to printed circuit boards. The exceptional thermal characteristics of this package depend entirely upon proper mechanical attachment.

Figure 37 depicts the package from the bottom and shows the dimensions of the exposed heat sink. A solid conduit of solder needs to be established between this pad and the surface of the PCB.

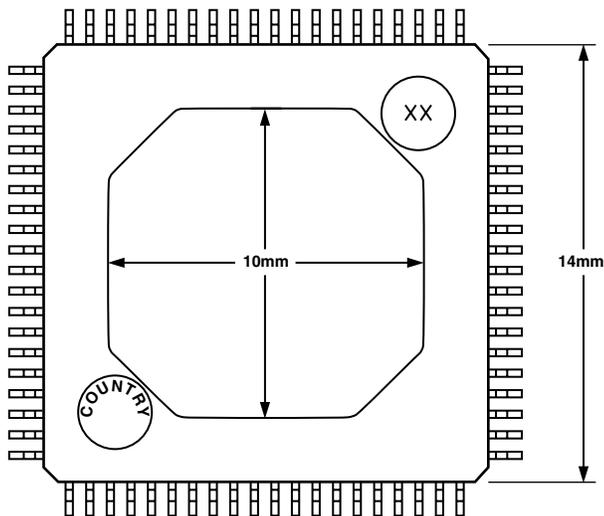


Figure 37.

Figure 38 depicts a general PCB land pattern for such an exposed heat sink device. Note that this pattern is for a 64-lead device, not an 80-lead, but the relative shapes and dimensions still apply. In this land pattern, a solid copper plane exists inside of the individual lands for device leads. Note also that the solder mask opening is conservatively dimensioned to avoid any assembly problems.

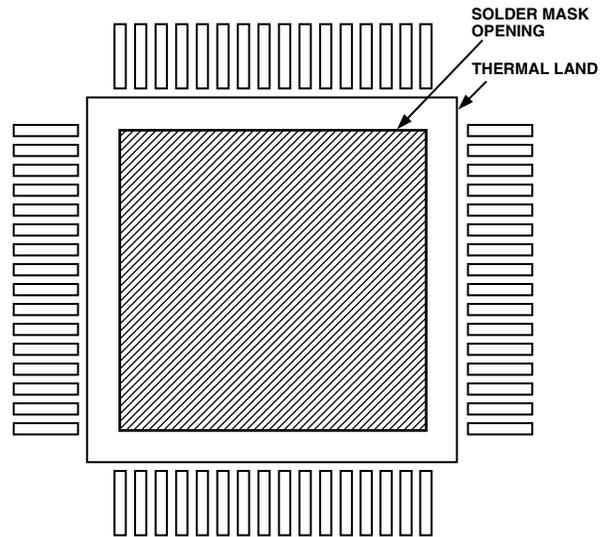


Figure 38.

The thermal land itself must be able to distribute heat to an even larger copper plane such as an internal ground plane. Vias must be uniformly provided over the entire thermal pad to connect to this internal plane. A proposed via pattern is shown in Figure 39. Via holes should be small (12 mil, 0.3 mm) such that they can be plated and plugged. These will provide the mechanical conduit for heat transfer.

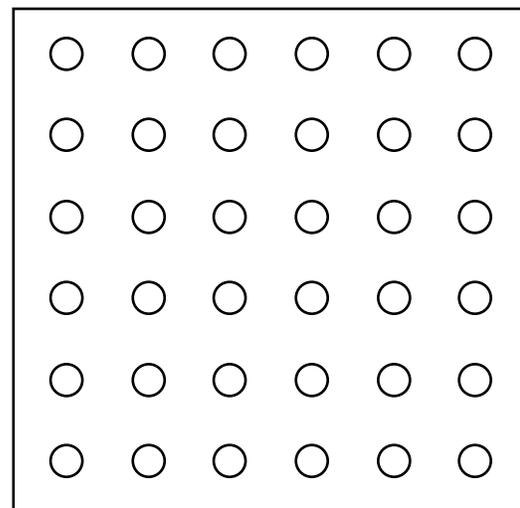


Figure 39.

Finally, a proposed stencil design is shown in Figure 40 for screen solder placement. Note that if vias are not plugged, wicking will occur, which will displace solder away from the exposed heat sink, and the necessary mechanical bond will not be established.

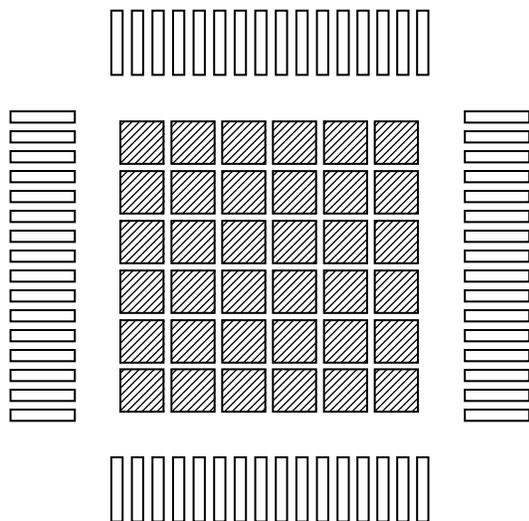


Figure 40.

EVALUATION BOARD

An evaluation board is available that supports the AD9852 DDS devices. This evaluation board consists of a PCB, software, and documentation to facilitate bench analysis of the performance of the AD9852 device. It is recommended that users of the AD9852 familiarize themselves with the operation and performance capabilities of the device with the evaluation board. The evaluation board should also be used as a PCB reference design to ensure optimum dynamic performance from the device.

EVALUATION BOARD INSTRUCTIONS

Introduction

The AD9852/AD9854 Rev E evaluation board includes either an AD9852ASQ or AD9854ASQ IC.

The ASQ package permits 300 MHz operation by virtue of its thermally enhanced design. This package has a bottom-side heat “slug” that must be soldered to the ground plane of the PCB directly beneath the IC. In this manner, the evaluation board PCB ground plane layer extracts heat from the AD9852/AD9854 IC package. If device operation is limited to 200 MHz and below, the AST package without a heat slug may be used in customer installations over the full temperature range. The AST package is less expensive than the ASQ package and those costs are reflected in the price of the IC.

Evaluation boards for both the AD9852 and AD9854 are identical except for the installed IC.

The AD9852 or AD9854 data sheet is essential to understanding all the modes of operation. While various *Preliminary* data sheets have been prepared and disseminated, only the released data sheet should be used since errors and omissions in the preliminary data sheets are inevitable. A released data sheet will have no Preliminary markings and will display a revision status such as “REV 0” or “REV A” at the lower left corner of each page.

To assist in proper placement of the pin-header shorting-jumpers, the instructions will refer to direction (left, right, top, bottom) as well as header pins to be shorted. Pin #1 for each three pin-header has been marked on the PCB corresponding with the schematic diagram. When following these instructions, position the PCB so that the PCB text can be read from left to right. The board is shipped with the pin-headers configuring the board as follows:

1. REFCLK for the AD9852/AD9854 is configured as differential. The differential clock signals are provided by the MC100LVEL16D differential receiver.
2. Input clock for the MC100LVEL16D is single-ended via J25. This signal may be 3.3 V CMOS or a 2 V p-p sine wave capable of driving 50 Ω (R13).
3. Both DAC outputs from the AD9852/AD9854 are routed through the two 120 MHz elliptical LP filters and their outputs connected to J7 (Q or Control DAC) and J6 (I or Cosine DAC).
4. The board is set up for software control via the printer port connector.
5. The DAC’s output currents are configured for 10 mA.

GENERAL OPERATING INSTRUCTIONS

Load the Version 1.71 software from the provided CD onto your PC’s hard disk. Connect a printer cable from the PC to the AD9852 Evaluation Board printer port connector labeled “J11.” Version 1.71 software will support Windows 95, Windows 98, and Windows NT.

Hardware Preparation: Using the schematic in conjunction with these instructions will be helpful in acquainting the user with the electrical functioning of the evaluation board.

Attach power wires to connector labeled “TB1” using the screw-down terminals. This is a plastic connector that press-fits over a 4-pin header soldered to the board. Table VIII shows connections to each pin. DUT = “device under test.”

Table VIII. Power Requirements for DUT Pins

AVDD 3.3 V	DVDD 3.3 V	VCC 3.3 V	Ground
All DUT Analog Pins	All DUT Digital Pins	All Other Devices	All Devices

Attach REFCLK to clock input, J25.

Clock Input, J25

This is actually a single-ended input that will be routed to the MC100LVEL16D for conversion to differential PECL output. This is accomplished by attaching a 2 V p-p clock or sine wave source to J25. Note that this is a 50 Ω impedance point set by R13. The input signal will be ac-coupled and then biased to the center-switching threshold of the MC100LVEL16D. To engage the differential-clocking mode of the AD9852, W3 Pins 2 and 3 (the bottom two pins) must be connected with a shorting jumper.

The signal arriving at the AD9852 is called the *Reference Clock*. If you choose to engage the on-chip PLL clock multiplier, this signal is the reference clock for the PLL and the multiplied PLL output becomes the *SYSTEM CLOCK*. If you choose to bypass the PLL clock multiplier, the reference clock that you have supplied is directly operating the AD9852 and is, therefore, the system clock.

Three-State Control

Three control or switch headers W9, W11, W12, W13, W14, and W15 must be shorted to allow the provided software to control the AD9852 evaluation board via the printer port connector J11.

AD9852

Programming

If programming of the AD9852 is not to be provided by the user's PC and ADI software, Headers W9, W11, W12, W13, W14, and W15 should be opened (shorting jumpers removed). This effectively detaches the PC interface and allows the 40-pin header, J10 and J1, to assume control without bus contention. Input signals on J10 and J1 going to the AD9852 should be 3.3 V CMOS logic levels.

Low-Pass Filter Testing

The purpose of 2-pin headers W7 and W10 (associated with J4 and J5) is to allow the two 50 Ω , 120 MHz filters to be tested during PCB assembly without interference from other circuitry attached to the filter inputs. *Normally, a shorting jumper will be attached to each header to allow the DAC signals to be routed to the filters.* If the user wishes to test the filters, the shorting jumpers at W7 and W10 should be removed and 50 Ω test signals applied at J4 and J5 inputs to the 50 Ω elliptic filters. User should refer to the provided schematic and the following sections to properly position the remaining shorting jumpers.

Observing the Unfiltered IOUT1 and the Unfiltered IOUT2 DAC Signals

This allows the viewer to observe the unfiltered DAC outputs at J5 (the "I" or Cosine signal) and J4 (the "Q" or Control DAC signal). The procedure below simply routes the two 50 Ω terminated analog DAC outputs to the SMB connectors and disconnects any other circuitry. The "raw" DAC outputs may appear as a series of quantized (stepped) output levels that may not resemble a sine wave until they have been filtered. The default 10 mA output current will develop a 0.5 V p-p signal across the on-board 50 Ω termination. If your "observation" equipment offers 50 Ω inputs, the DAC will develop only 0.25 V p-p due to the double termination.

1. Install shorting jumpers at W7 and W10.
2. Remove shorting jumper at W16.
3. Remove shorting jumper from 3-pin header W1.
4. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W4.

If using the AD9852 evaluation board, IOUT2, the Control DAC output is under user control through the serial or parallel ports. The 12-bit, two's-complement value(s) is/are written to the Control DAC register that will set the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum) with all zeros being midscale. Rapidly changing the contents of the Control DAC register (up to 100 MSPS) allows IOUT2 to assume any waveform that can be programmed.

Observing the Filtered IOUT1 and the Filtered IOUT2

This allows the viewer to observe the filtered "I" and "Q" (or Control) DAC outputs at J6 (the "I" signal) and J7 (the "Q" or Control signal). This places the 50 Ω (input and output Z) low-pass filters in the "I" and "Q" (or Control) DAC pathways to remove images and aliased harmonics and other spurious signals above approximately 120 MHz. For "I" and "Q" signals, these signals will appear as nearly pure sine waves and 90 degrees out-of-phase with each other. These filters are designed with the assumption that the system clock speed is at or near maximum (300 MHz). If your system clock speed is much less than 300 MHz, for example 200 MHz, it is possible or inevitable that unwanted DAC products other than the fundamental signal will be passed by the low-pass filters.

If you are using the AD9852 evaluation board, any reference to the "Q" signal should be interpreted to mean "Control DAC."

1. Install shorting jumpers at W7 and W10.
2. Install shorting jumper at W16.
3. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W1.
4. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W4.
5. Install shorting jumper on Pins 2 and 3 (bottom two pins) of 3-pin header W2 and W8.

Observing the Filtered IOUT1 and the Filtered IOUT1B

This allows the viewer to observe only the filtered "I" DAC outputs at J6 (the "true" signal) and J7 (the "complementary" signal). This places the 120 MHz low-pass filters in the true and complementary outputs paths of the "I" DAC to remove images and aliased harmonics and other spurious signals above approximately 120 MHz. These signals will appear as nearly pure sine waves and 180 degrees out-of-phase with each other. If your system clock speed is much less than 300 MHz, for example 200 MHz, it is possible or inevitable that unwanted DAC products other than the fundamental signal will be passed by the low-pass filters.

1. Install shorting jumpers at W7 and W10.
2. Install shorting jumper at W16.
3. Install shorting jumper on Pins 2 and 3 (top two pins) of 3-pin header W1.
4. Install shorting jumper on Pins 2 and 3 (top two pins) of 3-pin header W4.
5. Install shorting jumpers on Pins 2 and 3 (bottom two pins) of 3-pin header W2 and W8.

To Connect the High-Speed Comparator

To connect the high-speed comparator to the DAC output signals, either the quadrature filtered output configuration (AD9854 only) or the complementary filtered output configuration outlined above (both AD9854 and AD9852) can be chosen. Follow Steps 1 through 4 for either filtered configuration as above. Step 5 below will reroute the filtered signals away from their output connectors (J6 and J7) and to the 100 Ω configured comparator inputs. This sets up the comparator for *differential input without control of the comparator output duty cycle*. The comparator output duty cycle should be close to 50% in this configuration.

5. Install shorting jumper on Pins 1 and 2 (top two pins) of 3-pin header W2 and W8.

User may elect to change the R_{SET} resistor, R2 from 3.9 k Ω to 1.95 k Ω to receive a more robust signal at the comparator inputs. This will decrease jitter and extend comparator-operating range. User can accomplish this by installing a shorting jumper at W6, which provides a second 3.9 k Ω chip resistor (R20) in parallel with the provided R2. This boosts the DAC output current from 10 mA to 20 mA and doubles the p-p output voltage developed across the loads.

Single-Ended Configuration

To connect the high-speed comparator in a single-ended configuration that will allow duty cycle or pulsewidth control requires that a dc threshold voltage be present at one of the comparator inputs. You may supply this voltage using the control DAC. A 12-bit,

two's complement value is written to the Control DAC register that will set the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum) with all zeros being midscale. The IOUT1 channel will continue to output a filtered sine wave programmed by user. These two signals are routed to the comparator using W2 and W8 3-pin header switches. User must be in the configuration described in the section "Observing the Filtered IOUT1 and the Filtered IOUT2." Follow Steps 1 through 4 in that section and then the following:

5. Install shorting jumper on Pins 1 and 2 (top two pins) of 3-pin header W2 and W8.

The user may elect to change the R_{SET} resistor, R2 from 3.9 k Ω to 1.95 k Ω to receive a more robust signal at the comparator inputs. This will decrease jitter and extend comparator-operating range. User can accomplish this by installing a shorting jumper at W6, which provides a second 3.9 k Ω chip resistor (R20) in parallel with the provided R2.

USING THE PROVIDED SOFTWARE

The software is provided on a CD. This brief set of instructions should be used in conjunction with the AD9852 or AD9854 data sheet and the AD9852/AD9854 Evaluation Board schematic.

Version 1.71 Software has been improved from previous versions in the following ways:

- Detects old versions of the software installed and gives option to uninstall them.
- Detects the Windows Platform (Windows 95, Windows 98, Windows NT).
- Installs the correct version of the software (Windows 95/98 or Windows NT).
- Detects if Windows NT has Service Pack 3 installed, and if it does not, gives the option to install it.
- Allows access to the data sheets for both products through hyperlinks. (The hyperlinks bring up the executable that is currently associated with Acrobat files.)

The CD-ROM contains the following:

- The AD9852/AD9854 Evaluation Software.
- Service Pack 3 for Windows NT. This is required for Visual Basic 6.0 applications to run on Windows NT 4.0.
- Acrobat Reader 4.0 for Windows 95/98 and Windows NT.

Several numerical entries, such as frequency and phase information, require that the ENTER key be pressed to register that information. So, for example, if a new frequency is input, the load button is hit, and nothing new happens, it is probably because the user neglected to press the enter key after typing the new frequency information.

1. Normal operation of the AD9852/AD9854 evaluation board begins with a *master reset*. Many of the default register values after reset are depicted in the software "control panel." The reset command sets the DDS output amplitude to minimum and 0 Hz, 0 phase-offset as well as other states that are listed in the AD9852/AD9854 Register Layout table in the data sheet.
2. The next programming block should be the "Reference Clock and Multiplier" since this information is used to determine the proper 48-bit frequency tuning words that will be entered and calculated later.
3. The output amplitude defaults to the 12-bit straight binary multiplier values of the "I or Cosine" multiplier register of 000hex and no output (dc) should be seen from the DAC. Set the multiplier amplitude in the *Output Amplitude window* to a substantial value, such as FFFhex. The digital multiplier may be bypassed by clicking the box "Output Amplitude is always Full-Scale," but experience has shown that doing so does not result in best SFDR. *Best SFDR, as much as 11 dB better*, is obtained by routing the signal through the digital multiplier and "backing off" on the multiplier amplitude. For instance, FC0 hex produces less spurious signal amplitude than FFFhex. It is an exploitable and repeatable phenomenon that should be investigated in your application if SFDR (spurious-free dynamic range) must be maximized. This phenomenon is more readily observed at higher output frequencies where good SFDR becomes more difficult to achieve.
4. Refer to this data sheet and evaluation board schematic to understand all the functions of the AD9852 available to the user and to gain an understanding of what the software is doing in response to programming commands.

Applications assistance is available for the AD9852, the AD9852/PCB evaluation board, and all other Analog Devices products. Please call 1-800-ANALOGD.

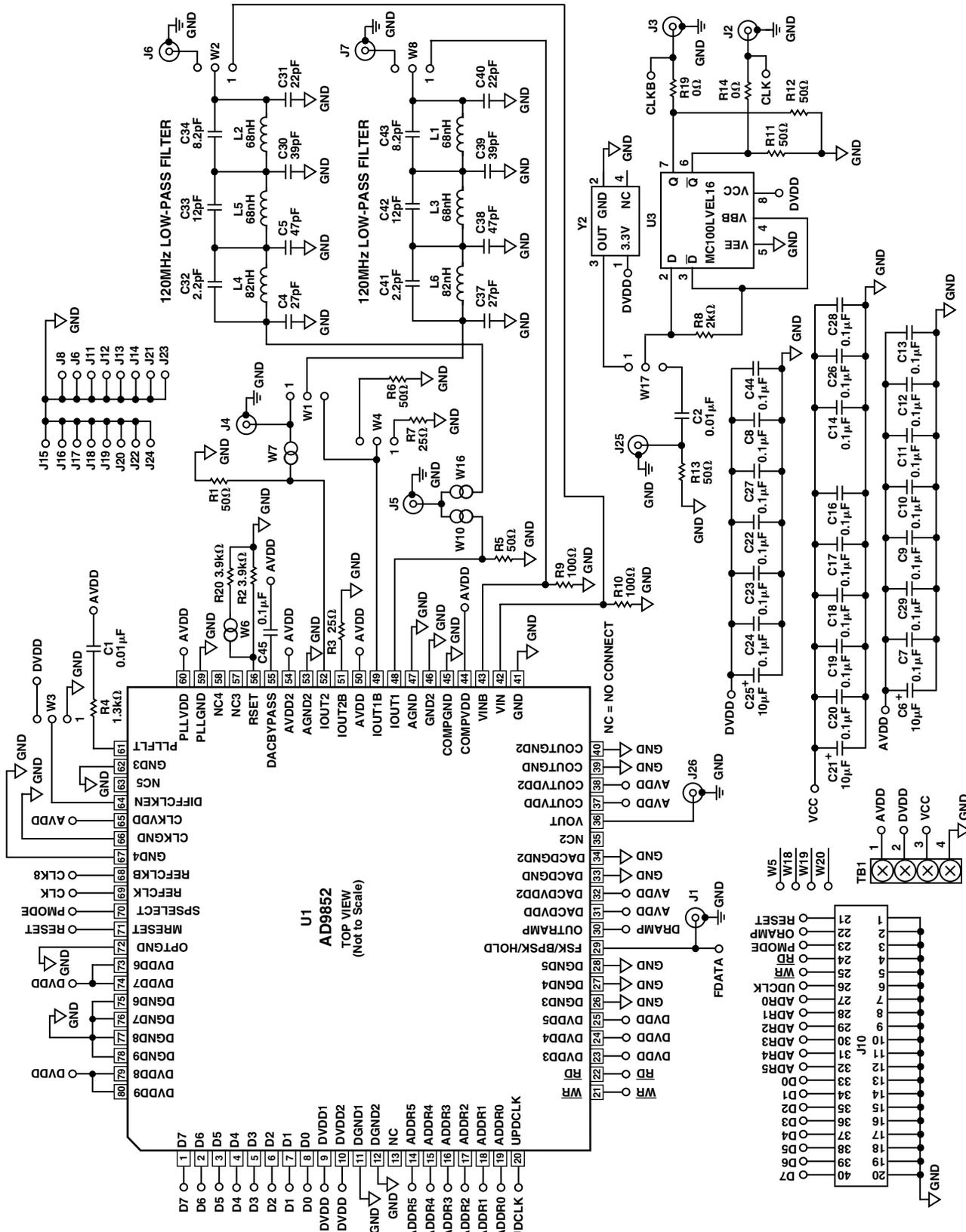


Figure 41a. Evaluation Board Schematic

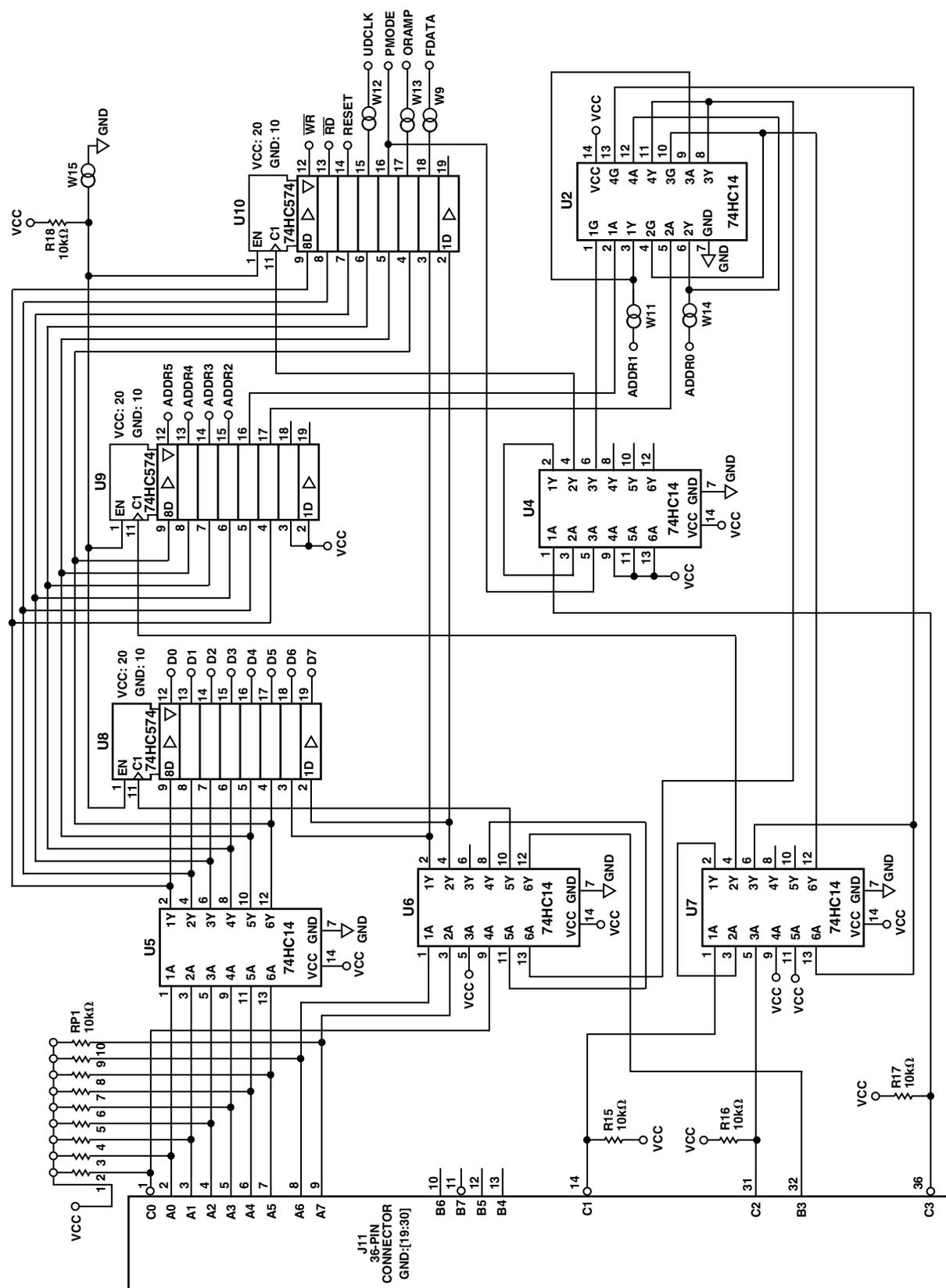


Figure 41b. Evaluation Board Schematic

AD9852

AD9852/54 Customer Evaluation Board
(AD9852 PCB > U1 = AD9852ASQ, AD9852 PCB > U1 = AD9852ASQ)

#	Quantity	REFDES	Device	Package	Value	Mfg. Part No.
1	3	C1, C2, C45	CAP	0805	0.01 μ F	
2	21	C7, C8, C9, C10, C11, C12, C13, C14, C16, C17, C18, C19, C20, C22, C23, C24, C26, C27, C28, C29, C44	CAP	0603	0.1 μ F	
3	2	C4, C37	CAP	1206	27 pF	
4	2	C5, C38	CAP	1206	47 pF	
5	3	C6, C21, C25	BCAPT	TAJD	10 μ F	
6	2	C30, C39	CAP	1206	39 pF	
7	2	C31, C40	CAP	1206	22 pF	
8	2	C32, C41	CAP	1206	2.2 pF	
9	2	C33, C42	CAP	1206	12 pF	
10	2	C34, C43	CAP	1206	8.2 pF	
11	9	J1, J2, J3, J4, J5, J6, J7 J25, J26	SMB	STR-PC MNT		ITT INDUSTRIES B51-351-000220
12	16	J8, J9, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24	W-HOLE			
13	1	J10	DUAL ROW HEADER	40 PINS		SAMTEC TSW-120-23-L-D
14	4	L1, L2, L3, L5	IND-COIL	1008CS	68 nH	COILCRAFT 1008CS-680XGBB
15	2	L4, L6	IND-COIL	1008CS	82 nH	COILCRAFT 1008CS-820XGBB
16	2	R2, R20	RES	1206	3900 Ω	
17	2	R3, R7	RES	1206	25 Ω	(24.9 Ω , 1%)
18	1	R4	RES	1206	1300 Ω	
19	4	R1, R5, R6, R11, R12, R13	RES	1206	50 Ω	(49.9 Ω , 1%)
20	1	R8	RES	1206	2000 Ω	
21	2	R9, R10	RES	1206	100 Ω	
22	4	R15, R16, R17, R18	RES	1206	10 k Ω	
23	1	RP1	RES NETWORK	SIP-10P	10 k Ω	Bourns 4610X-101-103
24	1	TB1	TERMINAL BLOCK & PINS	4-POSITION		WIELAND 25.602.2453.0 Block Z5.530.3425.0 Pins
25	1	U1	AD9852 or AD9852	80 LQFP		AD9852ASQ or AD9852ASQ
26	1	U2	74HC125	14 SO1C		SN74HC125D
27	1	U3	MC100LVEL16D	8 SO1C		MC100LVEL16D
28	4	U4, U5, U6, U7	74HC14	14 SO1C		SN74HC14D
29	3	U8, U9, U10	74HC574	20 SO1C		SN74HC574DW
30	1	J11	36 PIN CONNECTOR			AMP 552742-1
31	6	W1, W2, W3, W4, W8, W17	3-PIN JUMPER			SAMTEC
32	10	W6, W7, W9, W10, W11, W12, W13, W14, W15, W16	2-PIN JUMPER			SAMTEC
33	2		SELF-TAPPING SCREW	4-40, PHILIPS, ROUND HEAD		
34	4		RUBBER BUMPER	SQUARE BLACK		3M SJ-5018SPBL GSO2669 REV. E
35	1	AD9852/54 PCB				
36	2	R14, R19	0 Ω JUMPER	1206	0 Ω	
37	4		Pin Socket			AMP 5-330808-6
38	1	Y1 (Not Supplied)	XTAL	COSC		(Not Supplied)

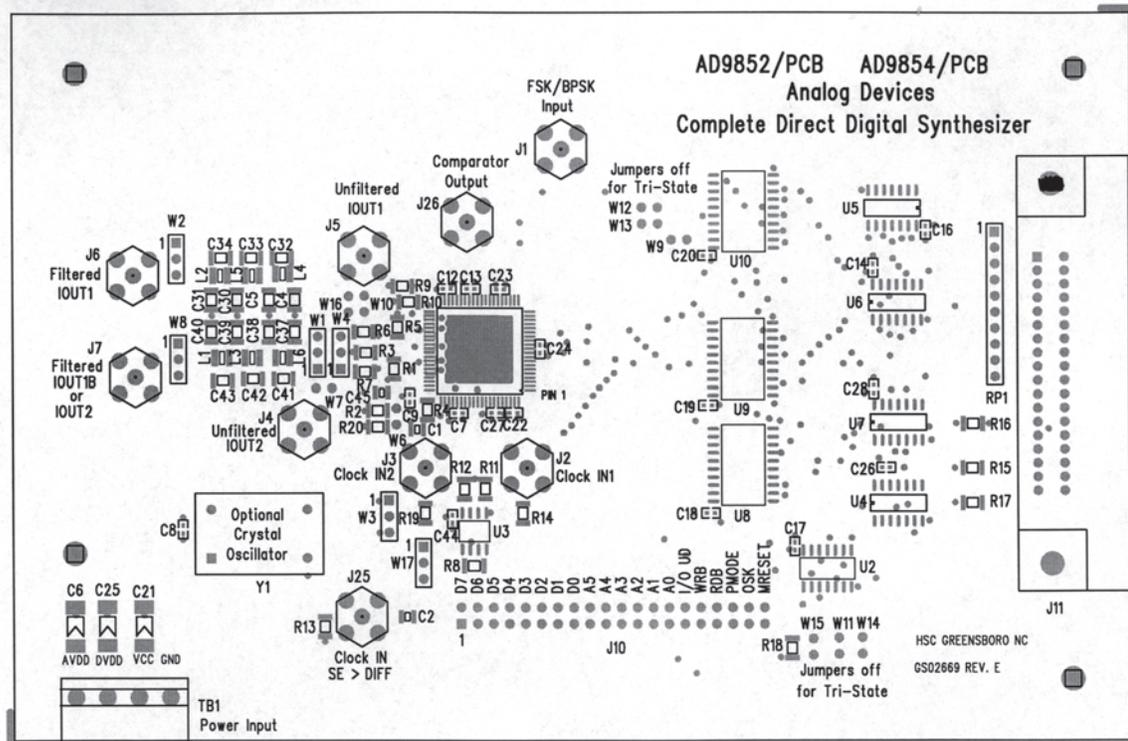


Figure 42. Assembly Drawing

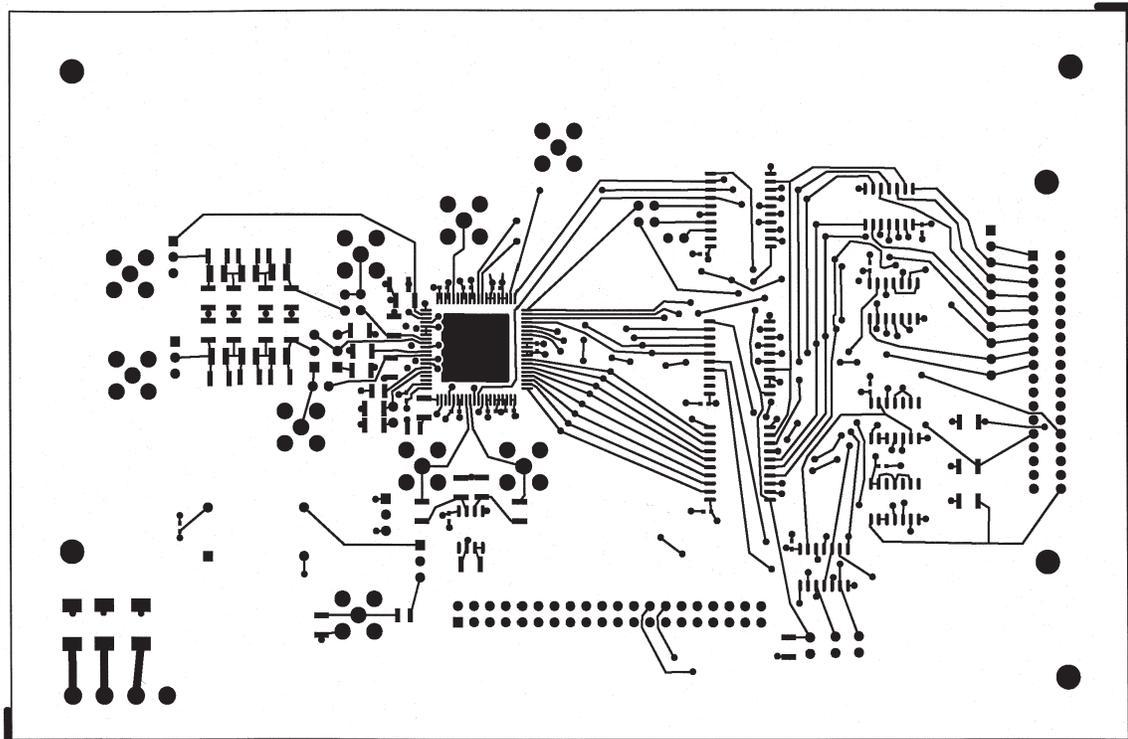


Figure 43. Top Routing Layer, Layer 1

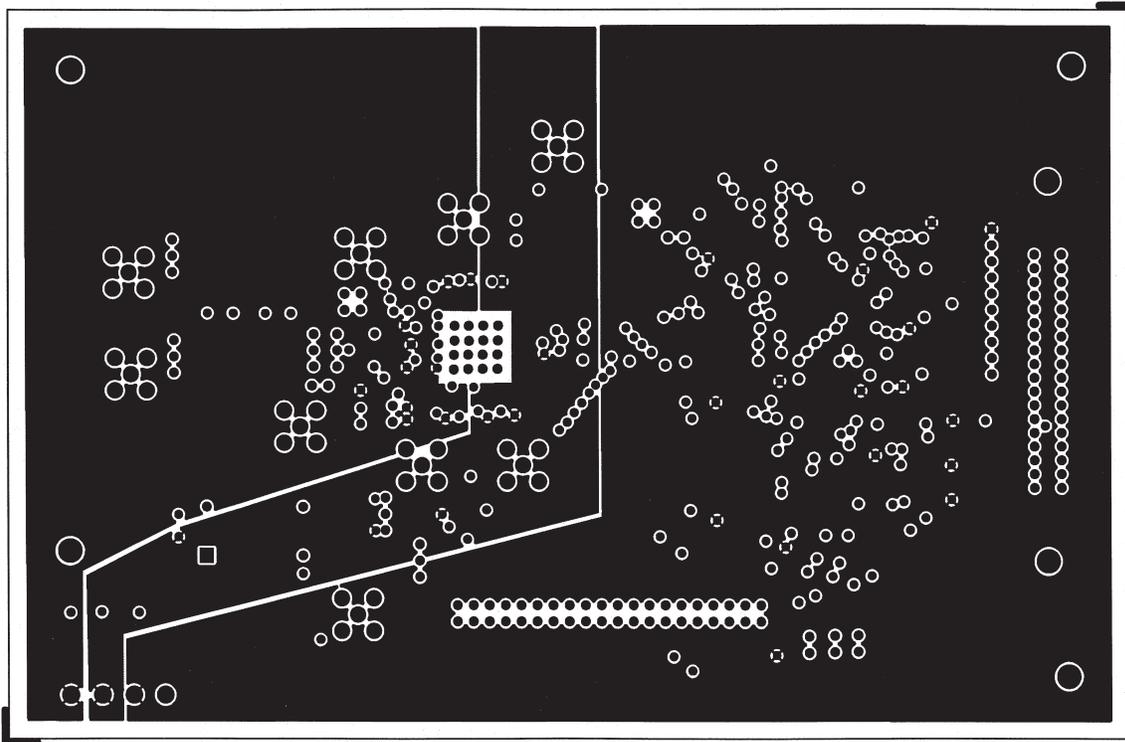


Figure 44. Ground Plane Layer, Layer 2

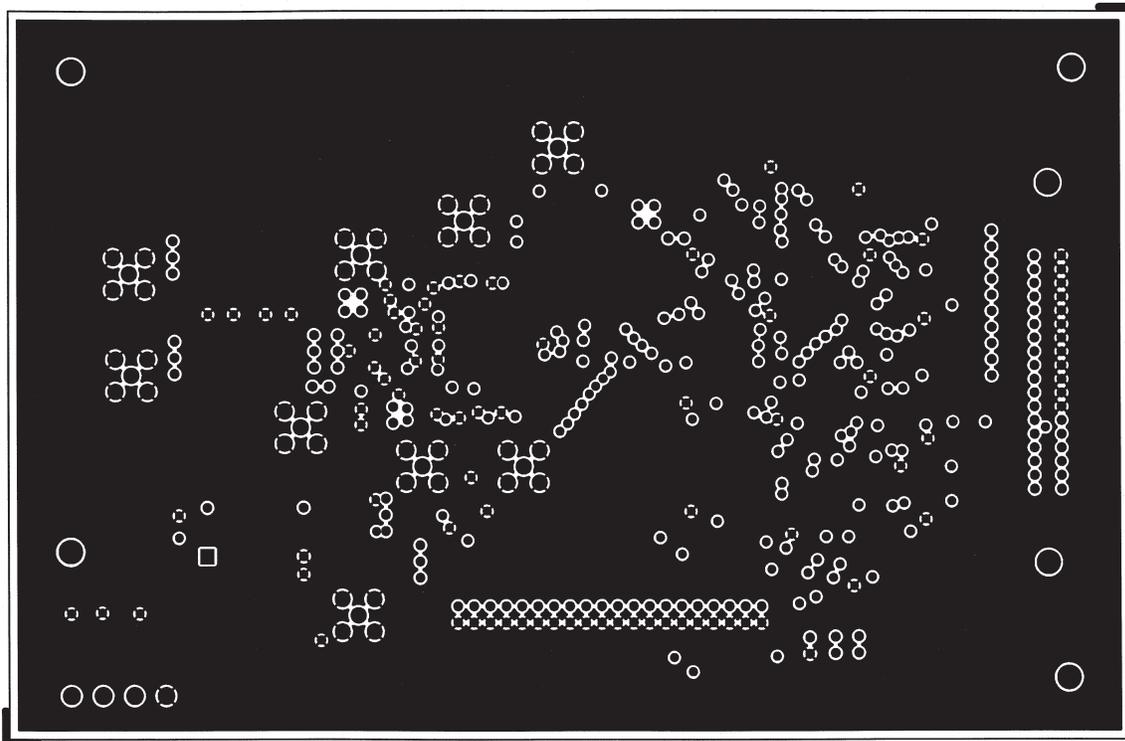


Figure 45. Power Plane Layer, Layer 3

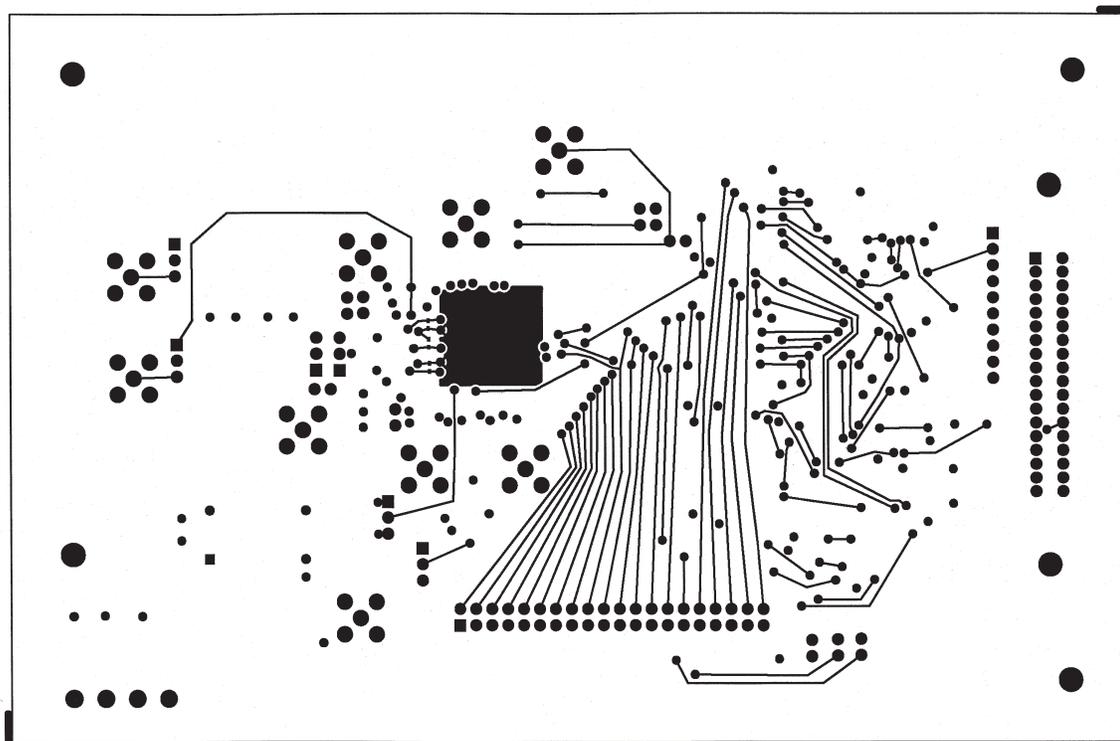
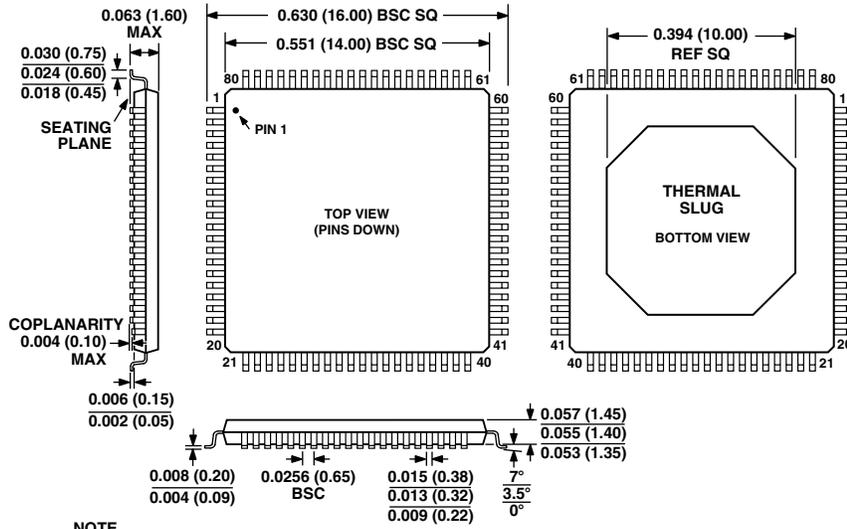


Figure 46. Bottom Routing Layer, Layer 4

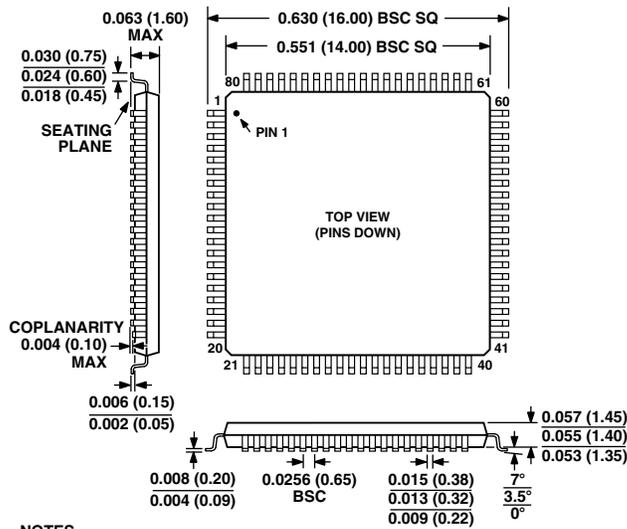
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

**80-Lead LQFP_ED
(SQ-80)**



NOTE
1. CENTER FIGURES ARE NOMINAL UNLESS OTHERWISE NOTED.

**80-Lead LQFP
(ST-80)**



NOTES
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. CENTER FIGURES ARE NOMINAL UNLESS OTHERWISE NOTED.

Revision History

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