



Preliminary Design Review: *SNS Normal Conducting Linac* *RF Control System*

Amy Regan

RF Controls Team:

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Rohlev, Dave Thomson, Yi-Ming Wang

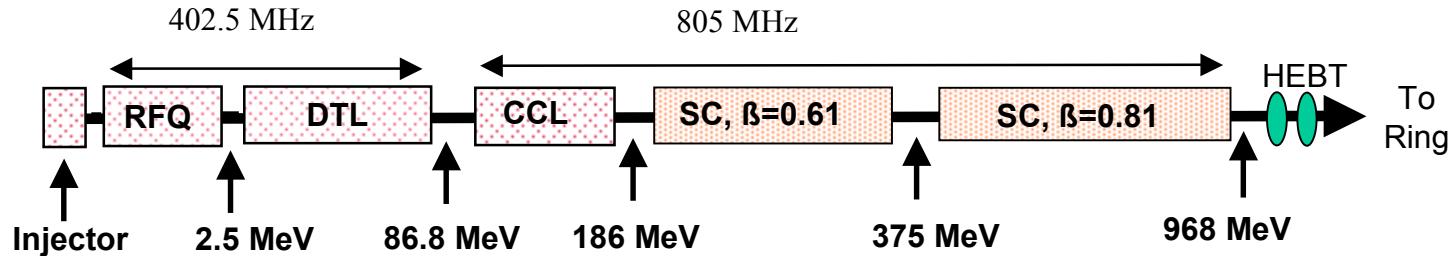
August 2, 2000

Agenda



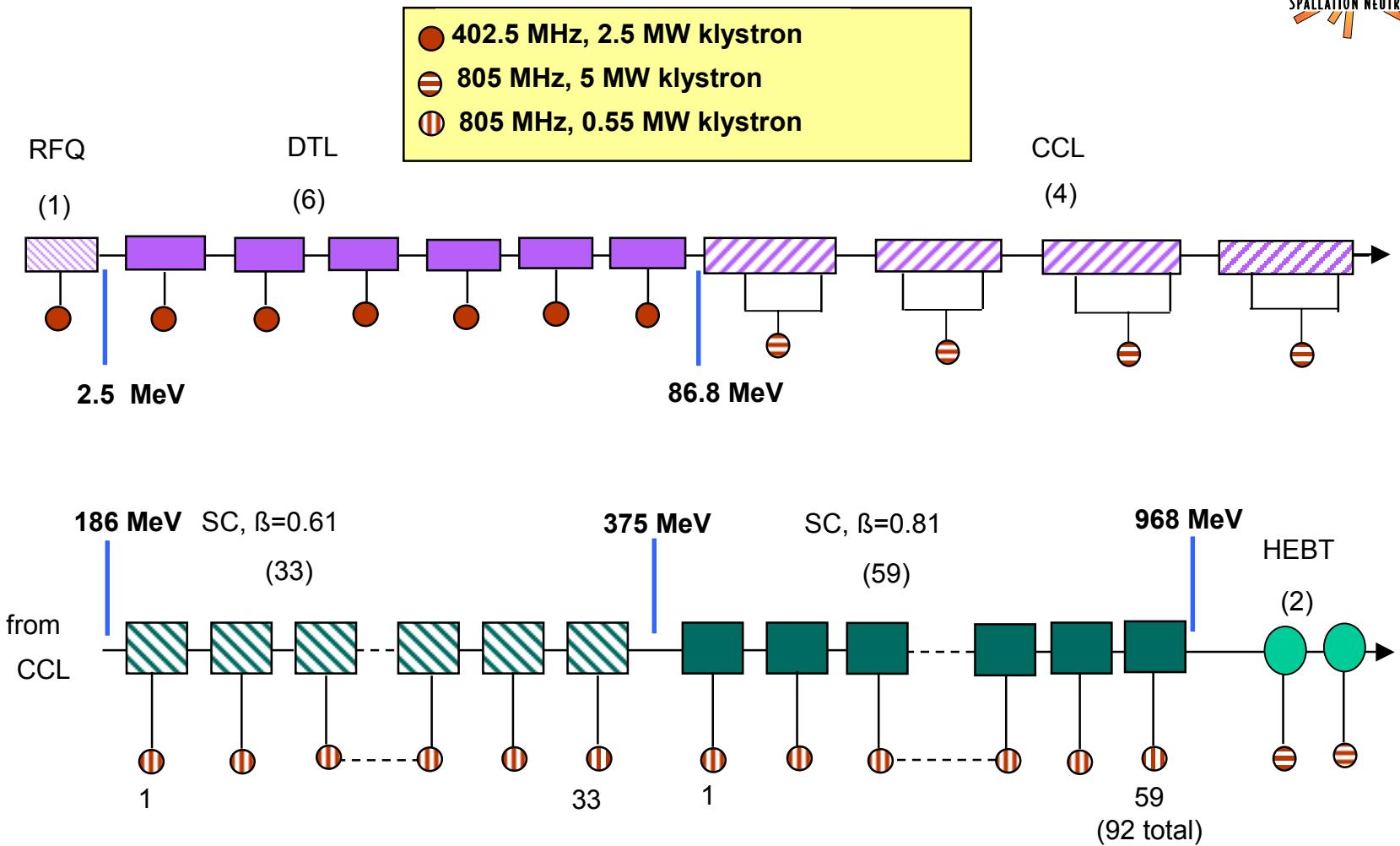
- 0. Top Level SNS Linac RF - RF Controls Specification (Regan)**
- 1. RF Control system design and implementation (Wang)**
- 2. Physical structure including Mother/Daughter layout. (Rohlev)**
 - 2a. RF/Analog section including Output stage and noise/distortion analysis (Rohlev)
 - 2b. Mother board including power layout and requirements etc. (Prokop)
 - 2c. PLD function and programs including PLD performance (Prokop)
 - 2d. DSP function and programs including memory layout (Wang)
- WORKING LUNCH**
- 3. Modeling and simulation (Kwon)**
- 4. HPRF Protect System (Thomson)**
- 5. Reference Distribution Design (Rohlev)**
- 6. Clock Distribution (Regan)**
- 7. Manufacturing plan (DeBaca)**
- 8. Global Controls Approach (Gurd)**
- 9. Cost and Schedule (Regan)**
- 10. Remaining Issues (Regan)**

NC/SC Linac for SNS

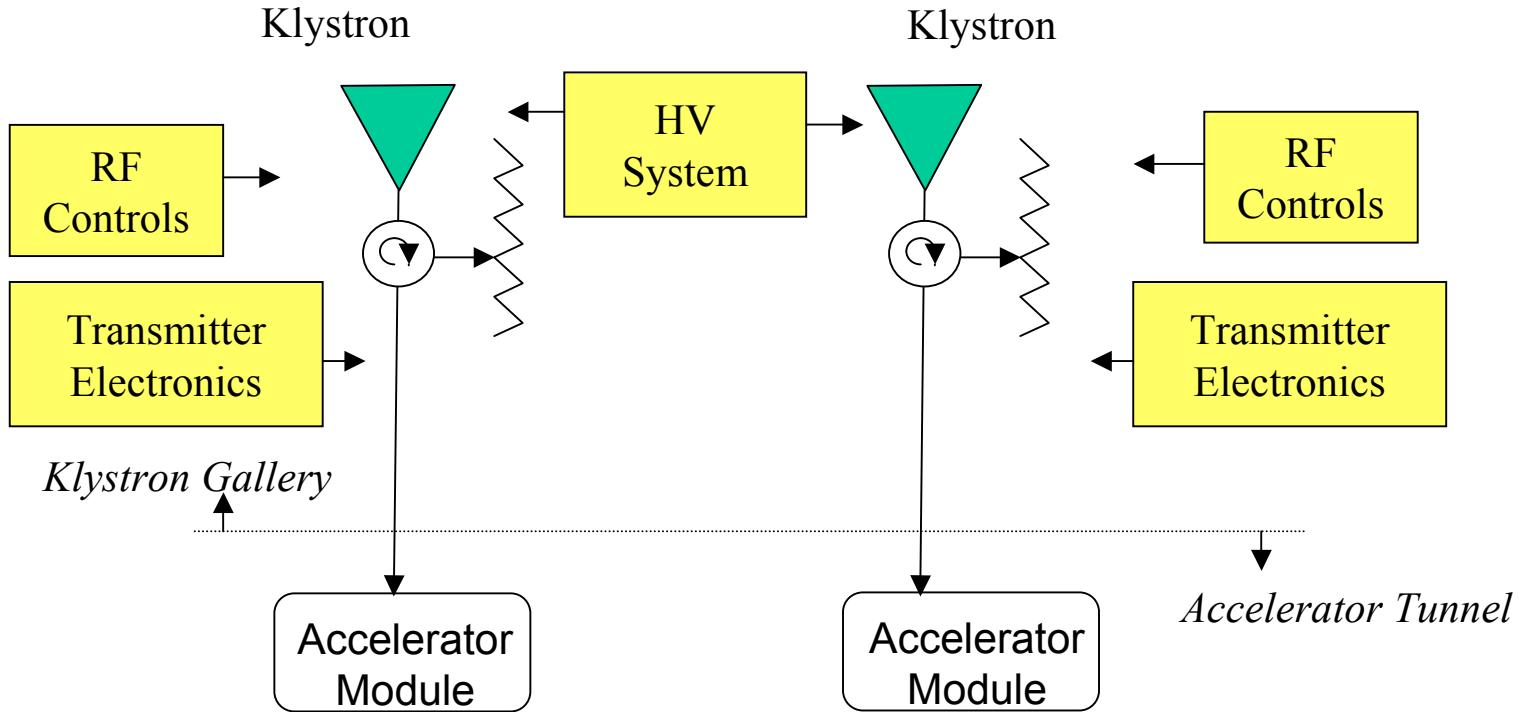


H-energy	968 MeV
Beam power	2 MW, avg.
Pulse Width	1.04 ms
Rep Rate	60 Hz
Klystrons	
402.5 MHz, 2.5 MW pk (iincludes 1 for RFQ, 6 for DTL)	7
805 MHz, 5 MW pk (iincludes 4 for CCL, 2 for HEBT)	6
805 MHz, 0.55 MW pk, SC	92
HV Converter/Modulator Systems	1 for each 5 MW klystron or pair of 2.5 MW klystrons except 1 for RFQ and first 2 DTL tanks and 1 for 2 HEBT cavities 1 for 11 or 12 each 0.55 MW klystrons (16 total, plus 2 for test stands)

Layout of Linac RF with NC and SC Modules

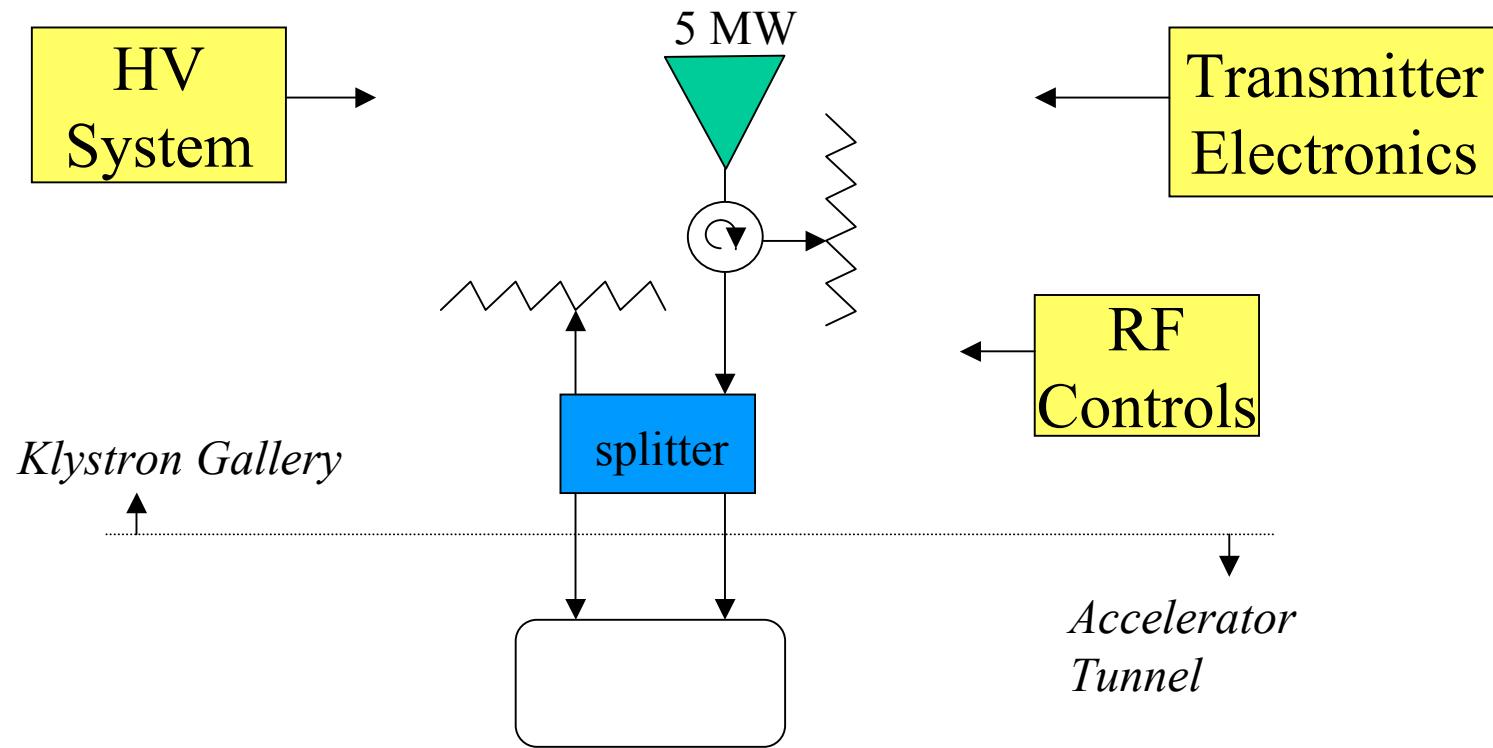


RF System Block Diagram, 2.5 MW klystrons, 402.5 MHz

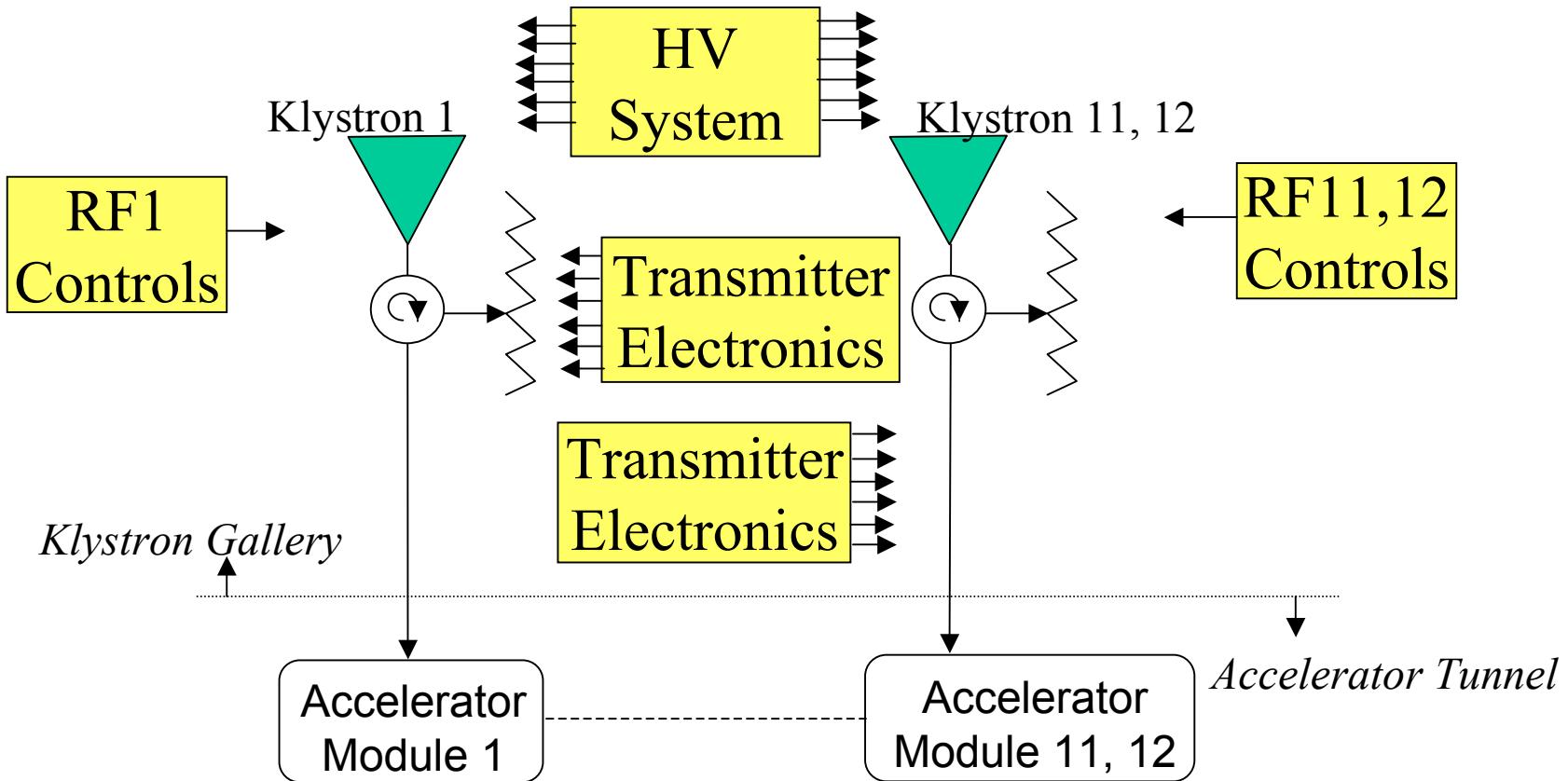


Note: The RFQ and the first 2 DTL tanks operate from one HV system

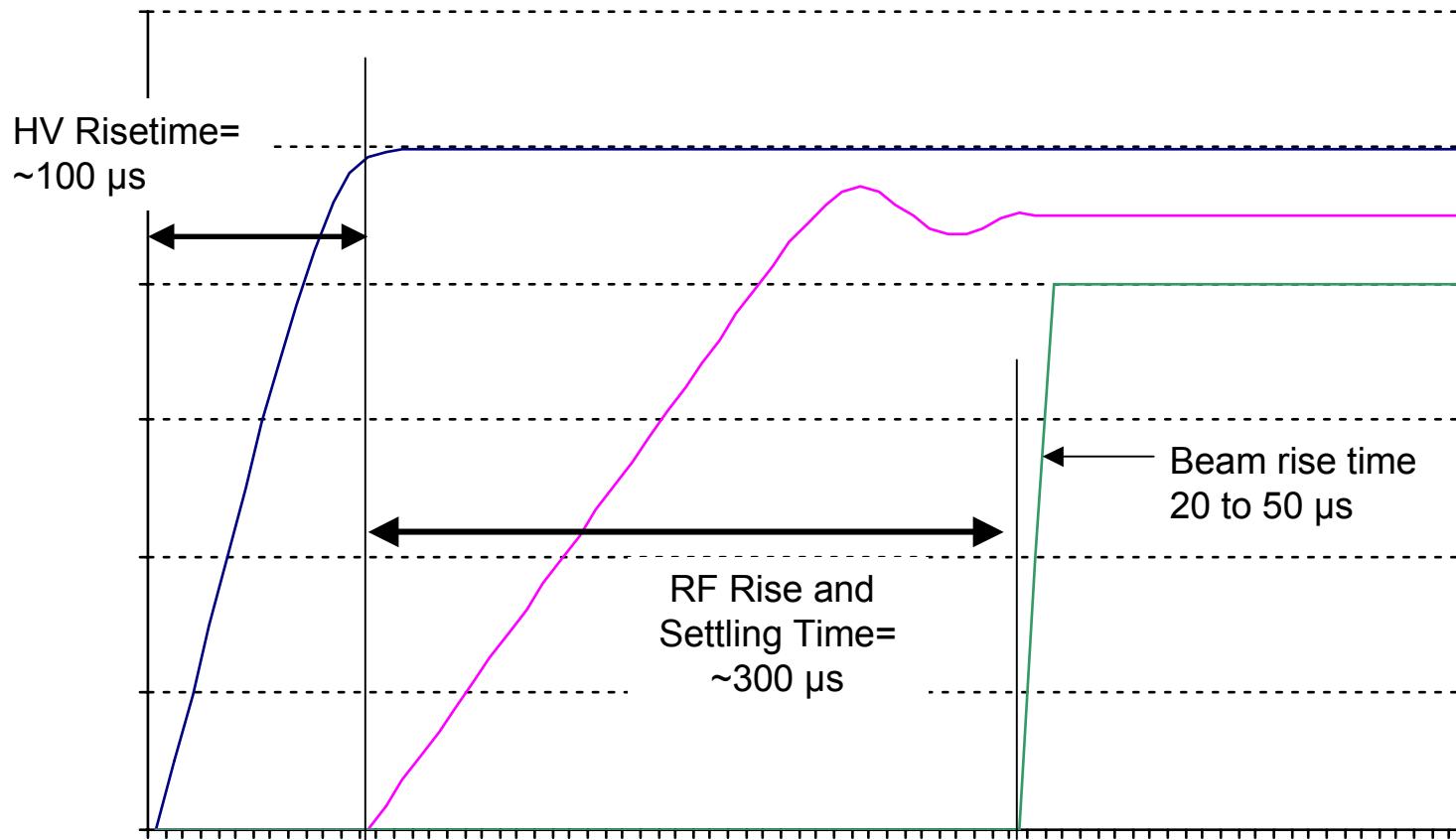
CCL RF Systems, 5 MW klystrons, 805 MHz



RF System Block Diagram, 0.55 MW klystrons, 805 MHz (SRF cavities)



Risetimes and Settling Times



RF control system requirements drive design



- REQUIRED FUNCTIONS
 - Cavity Field Control
 - Cavity Resonance Control
 - RF Reference generation and distribution
 - HPRF protection
- ANTICIPATED NC SYSTEM CONFIGURATIONS
 - Single 2.5 MW klystron driving single cavity (402.5 MHz)
 - Single 5 MW klystron driving single cavity through a split (805 MHz)
- ANTICIPATED OPERATIONAL & CONDITIONING SCENARIOS
 - Pulsed beam, Pulsed RF
 - 60 Hz rep rate
 - 68% chopping, 36 mA avg

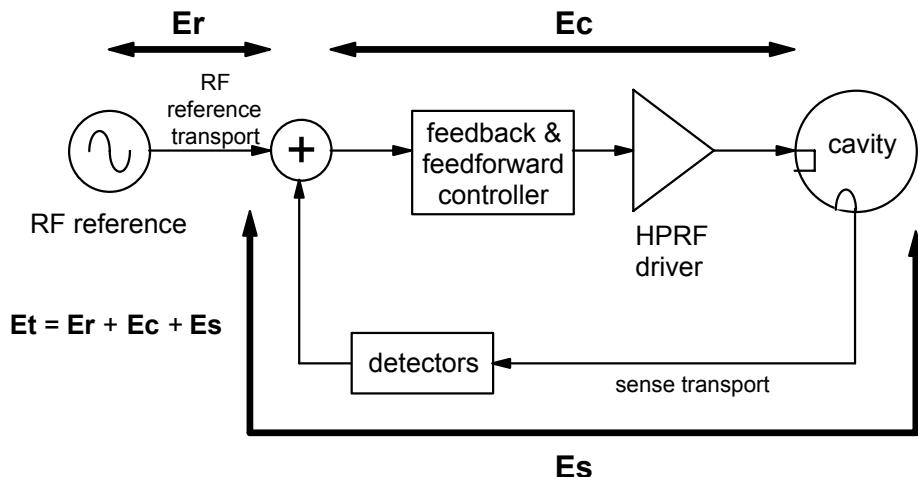
RF Control System Requirements (cont'd.)



CAVITY FIELD & RESONANCE CONTROL SPECIFICATIONS:

FIELD CONTROL $\pm 0.5\%$ amplitude, $\pm 0.5^\circ$ phase	A graph illustrating the field control specification. It shows two horizontal dashed lines representing the acceptable range of field amplitude. A solid black line represents the actual field measurement, which exhibits a sharp, transient dip (voltage drop) followed by a recovery. Arrows indicate the peak-to-peak amplitude of this transient dip. Labels next to the arrows specify the tolerance: $\pm 0.5\%, \pm 0.5^\circ$ for the initial dip, and $\pm 0.75\%, \pm 0.75^\circ$ for the subsequent recovery phase.
RESONANCE CONTROL Maintain cavity resonance	<p>402.5 MHz: RFQ ± 20 kHz ($Q_L = 3480$ $BW = 25$ kHz)</p> <p>402.5 MHz: DTL ± 4 kHz ($Q_L = 12,350$ $BW = 33$ kHz)</p> <p>@805 MHz: CCL ± 10 kHz ($Q_L = 9450$ (worst case) $BW = 85$ kHz)</p>

Error Allocation



E_r = reference line transport error

E_c = residual control loop error

E_s = sense line and detection error

E_t = total system error



PERFORMANCE OBJECTIVES

PEAK AMPLITUDE ERROR: $\leq 0.5\%$

PEAK PHASE ERROR: $\leq 0.5^\circ$

TOLERANCE BUDGET

-AMPLITUDE (%)

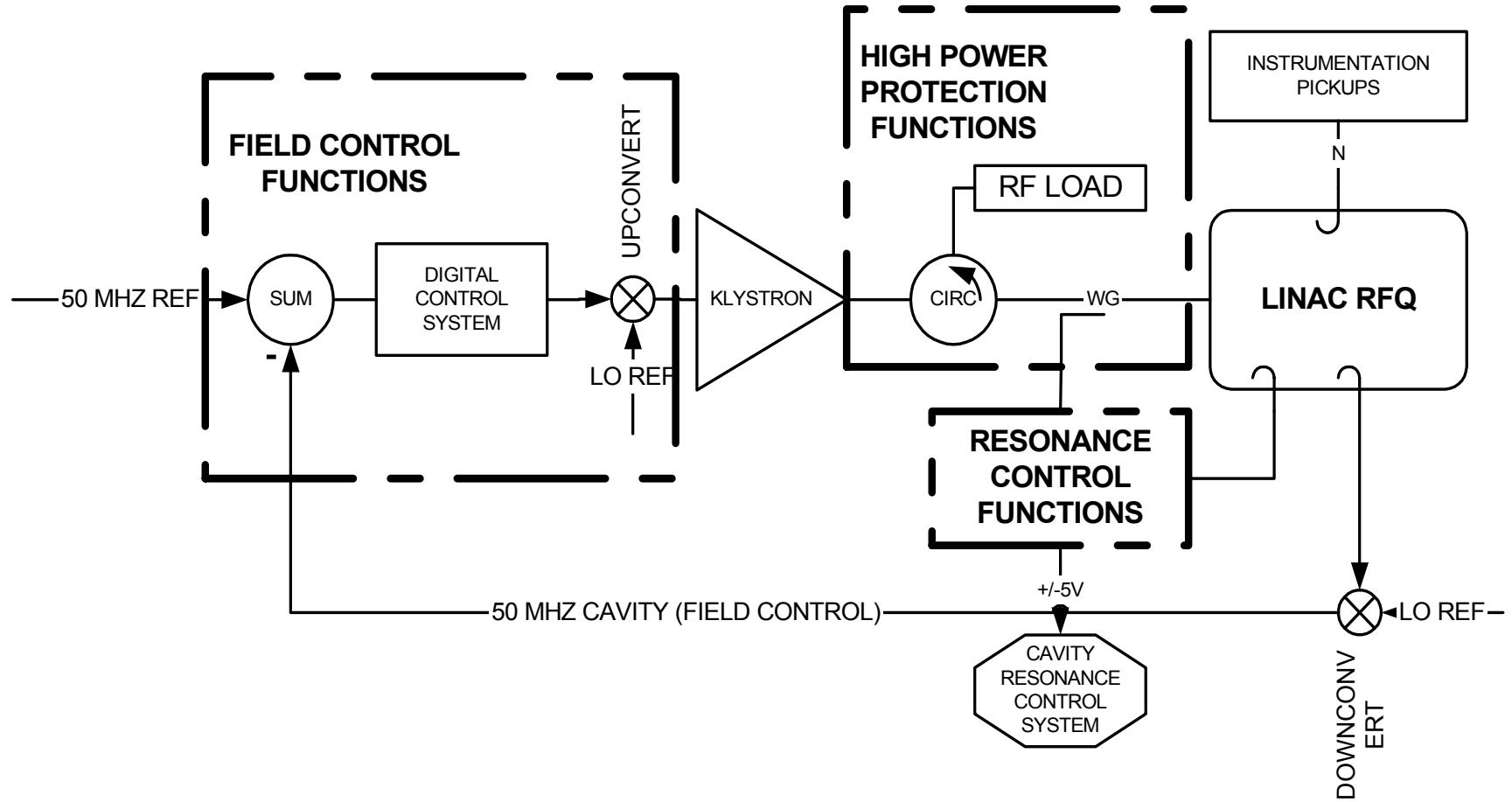
	PHASE
E_r	N/A
E_s	± 0.15
E_c	± 0.2

LEDA LESSONS LEARNED

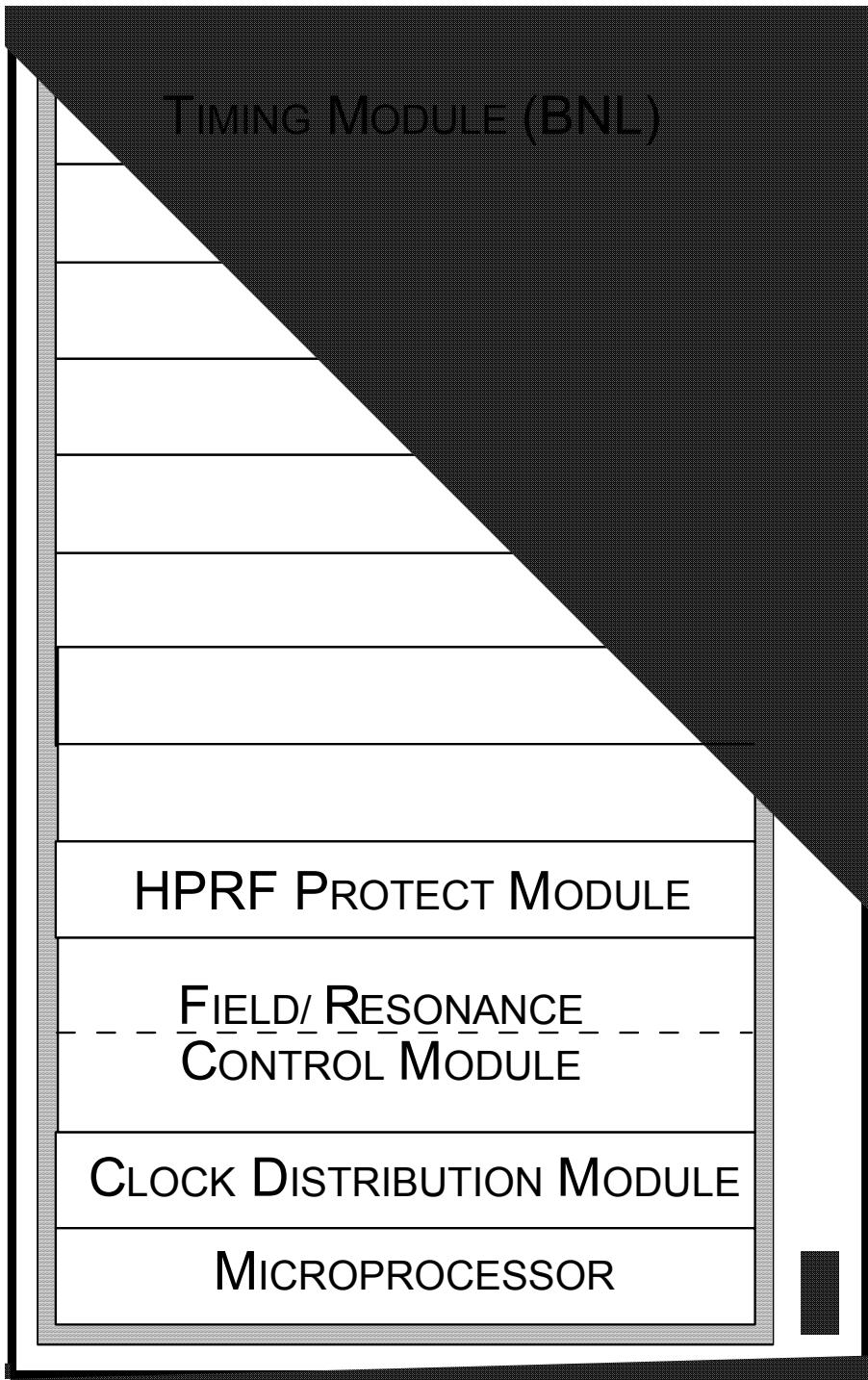


- FREQUENCY TRACKING - GET RID OF THE SIDEBANDS.
 - USE VCO FOR IF MODULATION RATHER THAN DDS
- TURN-ON TRANSIENT OVERSHOOT - HAS TO BE FASTER
 - NEW ALL DIGITAL DESIGN SHOULD GIVE US >100 kHz BW
- HPRF PROTECT - SHRINK NUMBER OF CHANNELS
 - STILL NEED BELLS AND WHISTLES BUT MAKE IT EASIER TO SET UP
- IN GENERAL, NEED BETTER REAL-TIME DIAGNOSTICS TO TELL WHAT'S GOING ON
 - PLAN TO INCORPORATE MORE FRONT PANEL TEST POINTS

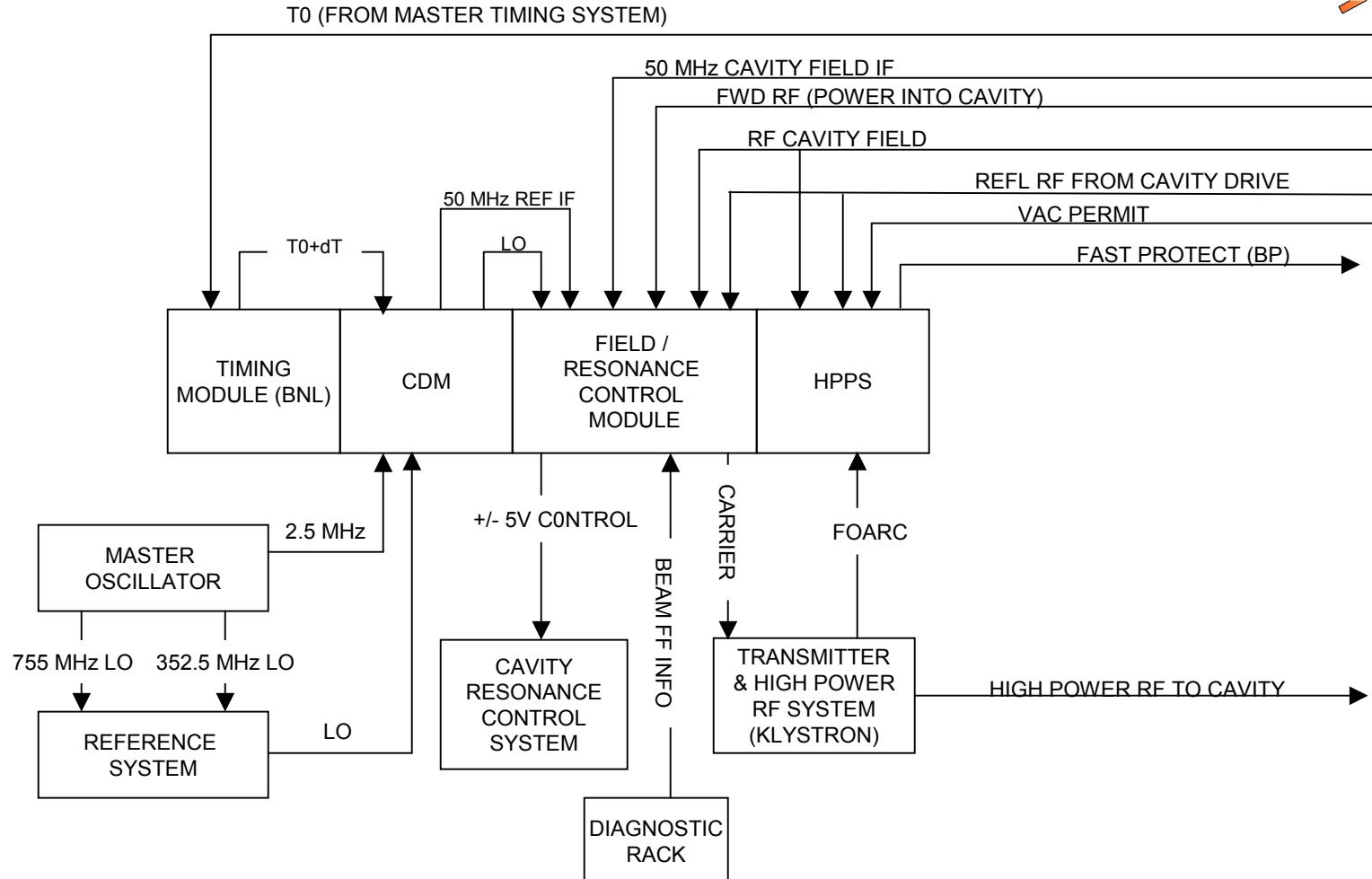
RFCS Functional Block Diagram



RF Control System VXIbus Crate



Interconnection Diagram





RF Controls Preliminary Design Review

DIGITAL CONTROL SYSTEM FOR SNS LLRF

Yi-Ming Wang

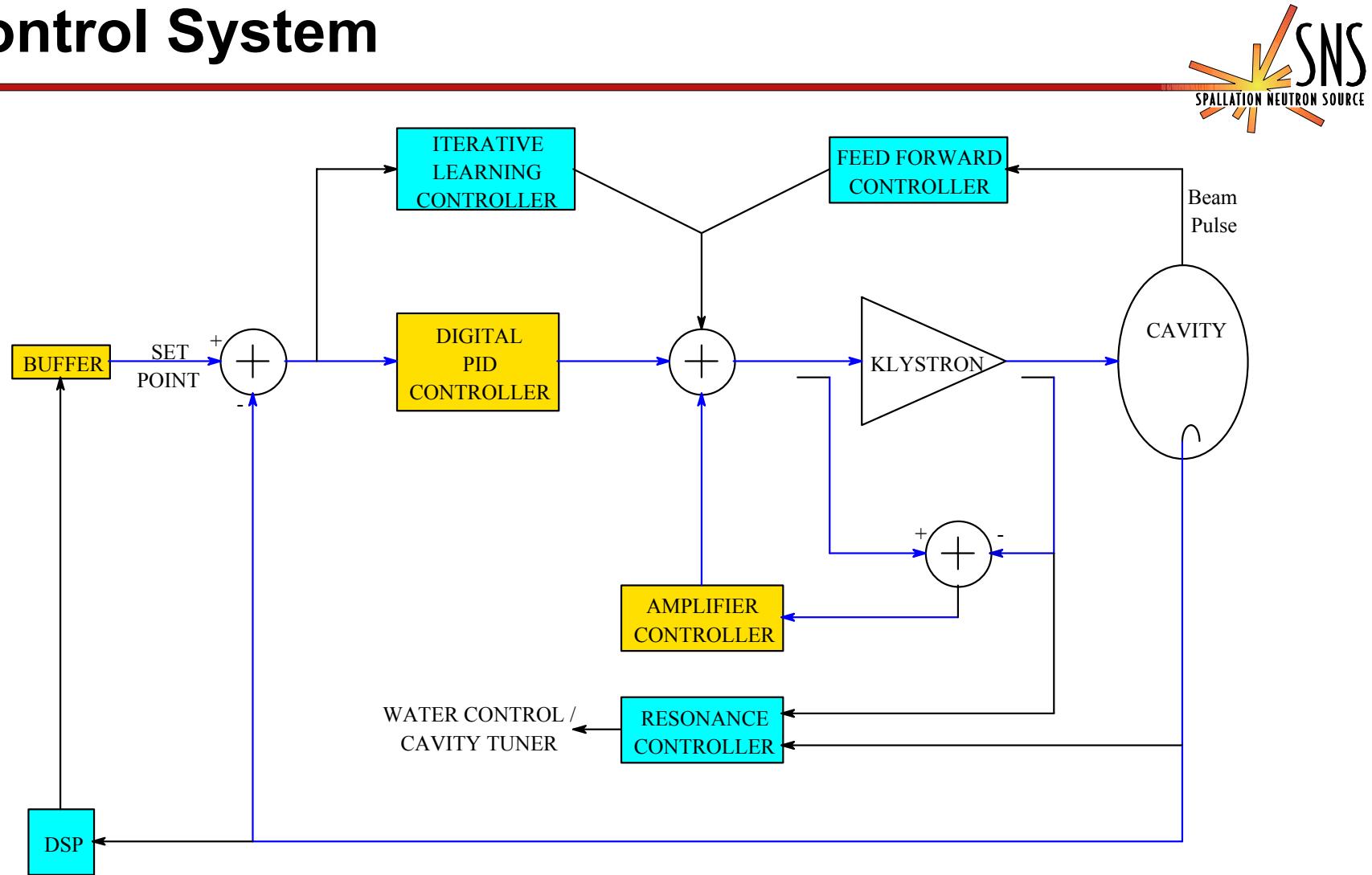
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DIGITAL FIELD CONTROL SYSTEM REQUIREMENTS



- Control Bandwidth: 200 kHz
- Latency of the signal path: 1 μ s
- Controllers: PID, Feed-Forward and other modern controllers.
- History buffers: Available along the signal paths
- Calibration: Real time auto calibration (beam off for a few pulses)

Functional Block Diagram of the Digital Control System



SYSTEM ARCHETECTURE OF FIELD AND RESONANT CONTROL MODULE FOR SNS LLRF



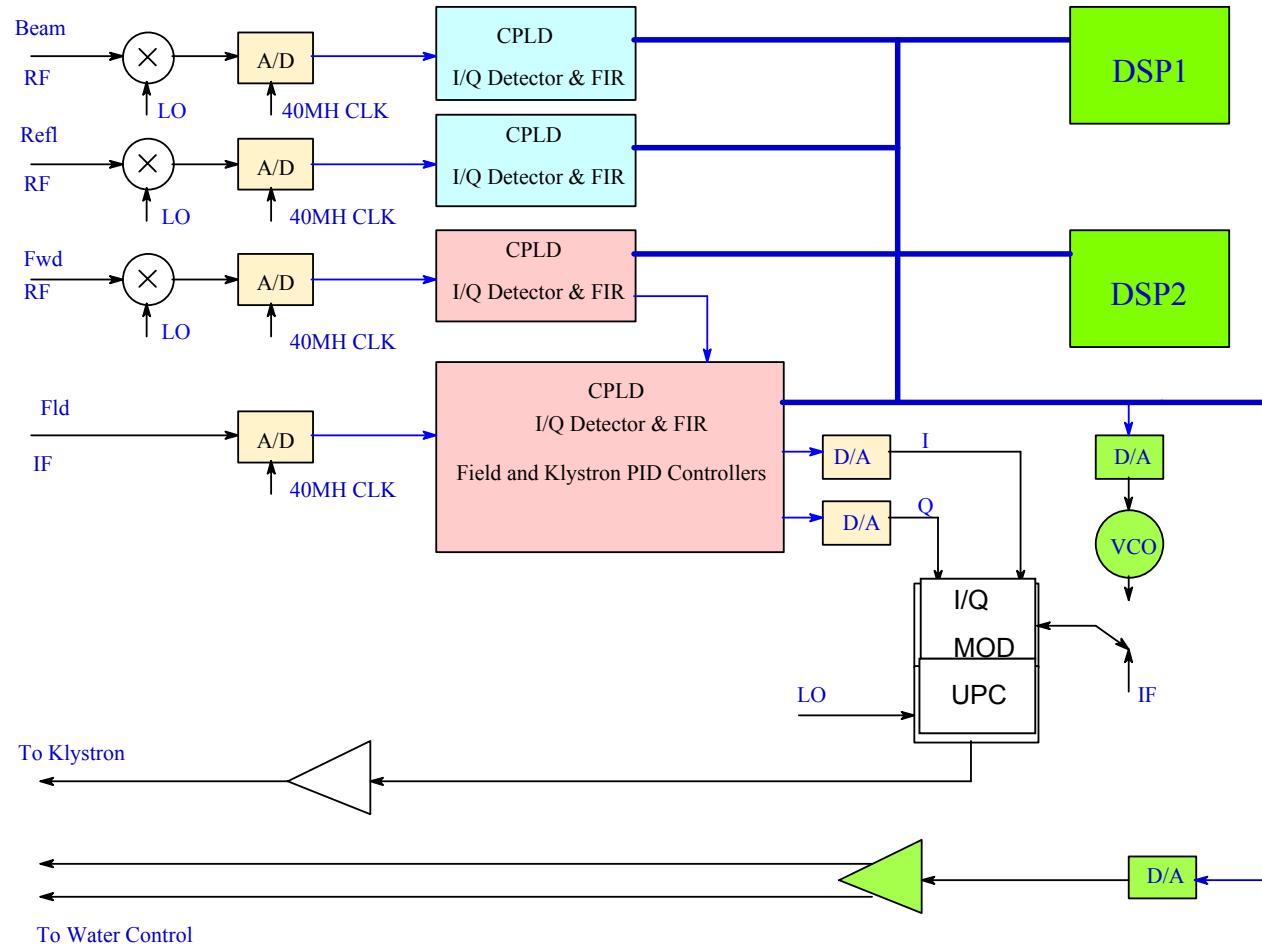
- A General Purpose MotherBoard Which provides VXI interface and Bus arbitration function for DSP and Front-Plug in board and could host two DSP plug-in boards and two Front-plug-in boards;
- Two DSPs: One DSP for Resonance Control and other for Field Control (adaptive feed forward and gain scheduling);
- One front-end-board for all RF I/O and Digital I/Q demodulation and fast digital control processing (Field control, resonant control and beam feed forward).
- Multi-rate digital processing in CPLD for optimized though-put in fast field control signal path.

Digital Control Board Functions and I/O



- Functions:
 - Field Control
 - Resonant Control
 - Beam Feed Forward
 - Klystron Control
- Input Signal:
 - Cavity field (IF 50MHz)
 - Forward field (RF)
 - Reflected field (RF)
 - LO and IF (50MHz)
 - Beam (RF)
- Output Signal:
 - RF to Klystron
 - Analog differential signal to water resonant control

Digital Control Module Block Diagram



Latency Estimation



- Fast Direct Signal Path: A/D-CPLD-D/A
- Latency of the direct signal path: (20 MHz clock)

A/D	I/Q Demod	FIR	PID	D/A	TOTAL	
2-3	1-2		1-11	1-2	1-2	6-21 (clk
cycles)						300-

1050(ns)

- DSP Functions: Supervisory, Mode control, Calibration, Adaptive gain control, Resonance Control, Beam(or Error) Feed-forward.

Others



- DIAGNOSTICS
 - Field magnitude measurement for all input signals (analog)
 - Digital signals along the signal path available through the history buffers
 - Two front analog test points (I/Q control out or any magnitude measurement)
- AUTO-CALIBRATION
 - Loop phase calibration during normal operation (with beam pulse off for few pulses)



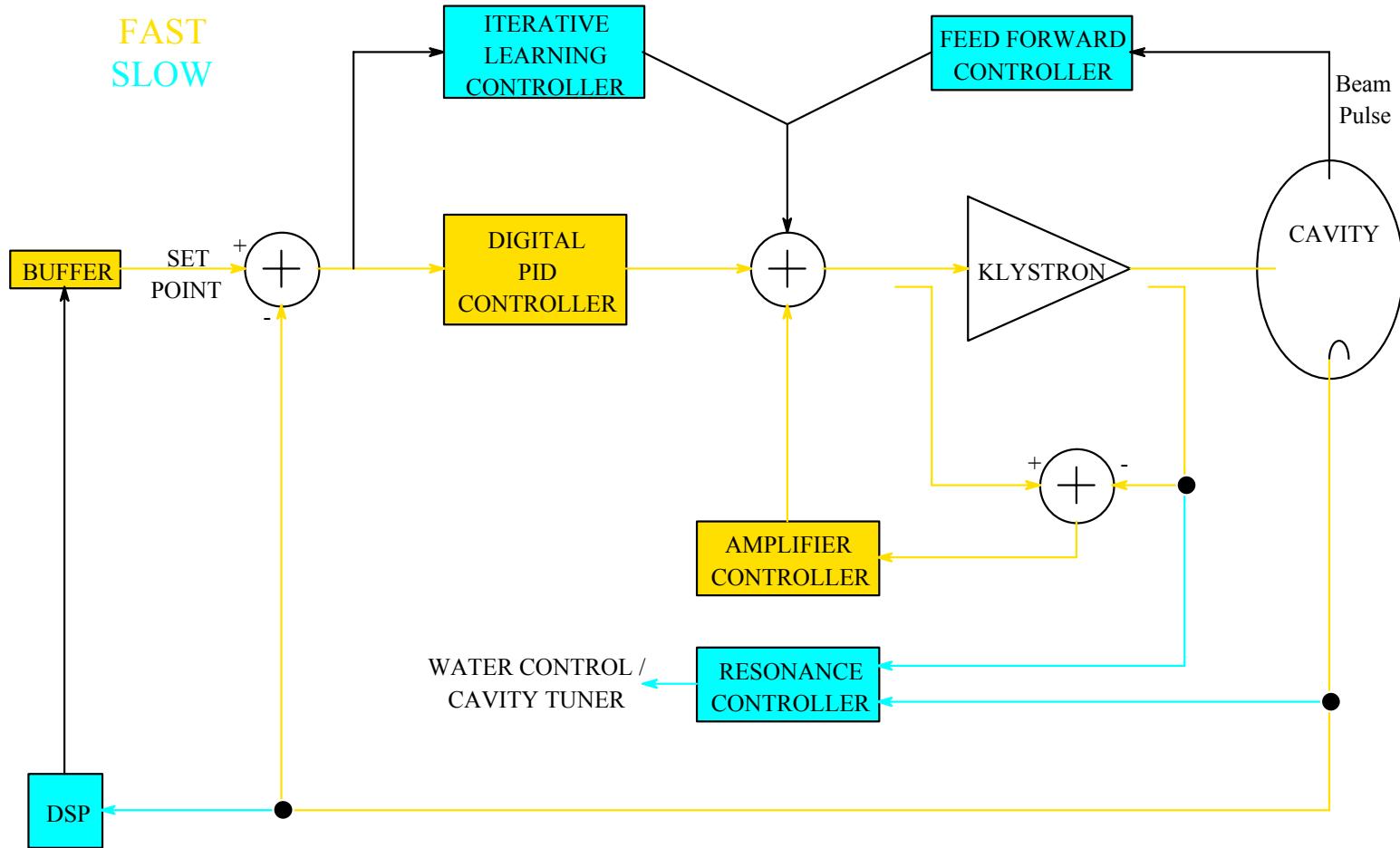
RF Controls Preliminary Design Review

SNS Control System RF/Analog Layout and Noise Analysis

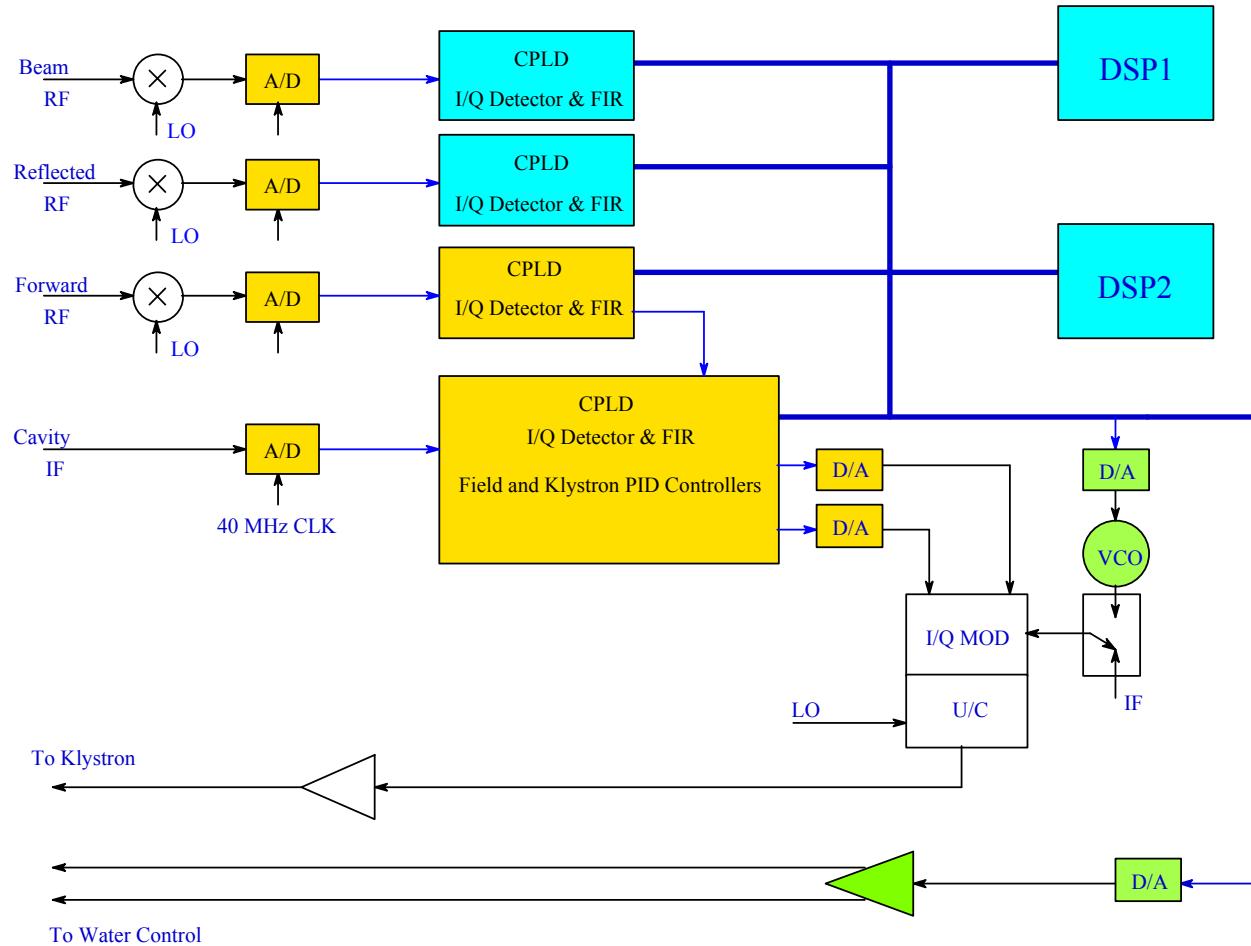
Tony Rohlev

August 2, 2000

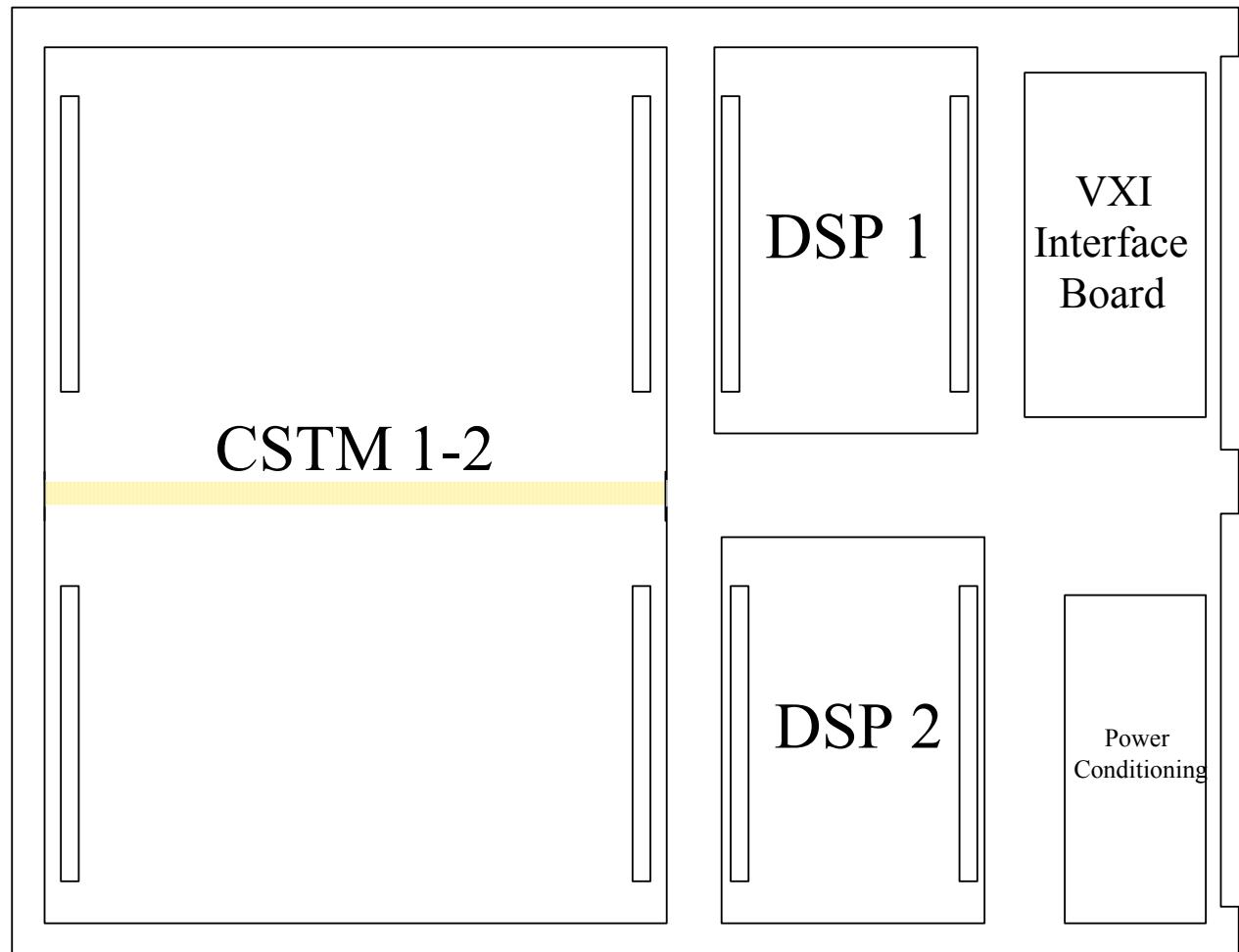
Simplified Block Diagram



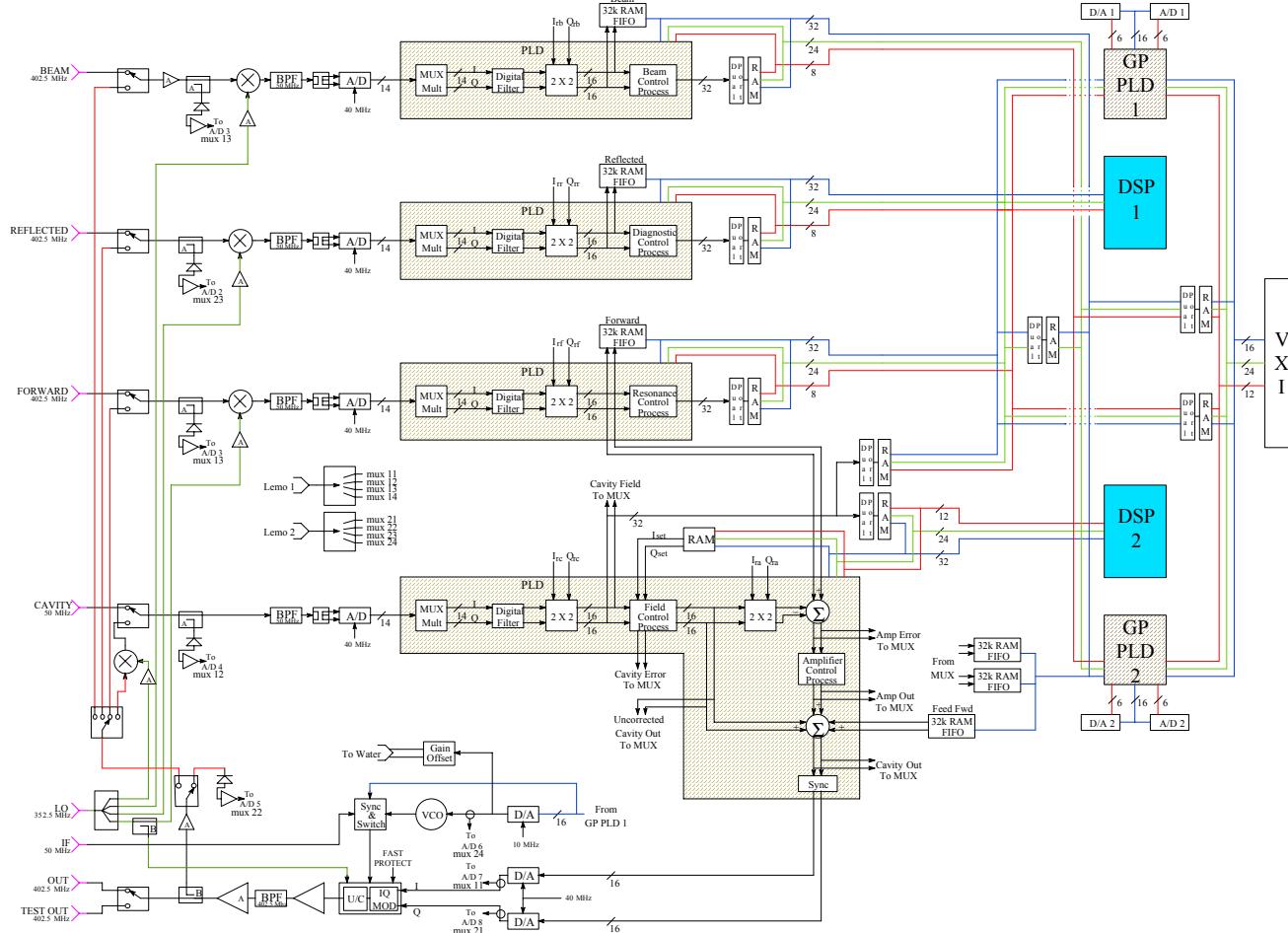
Simplified Control Board Functionality



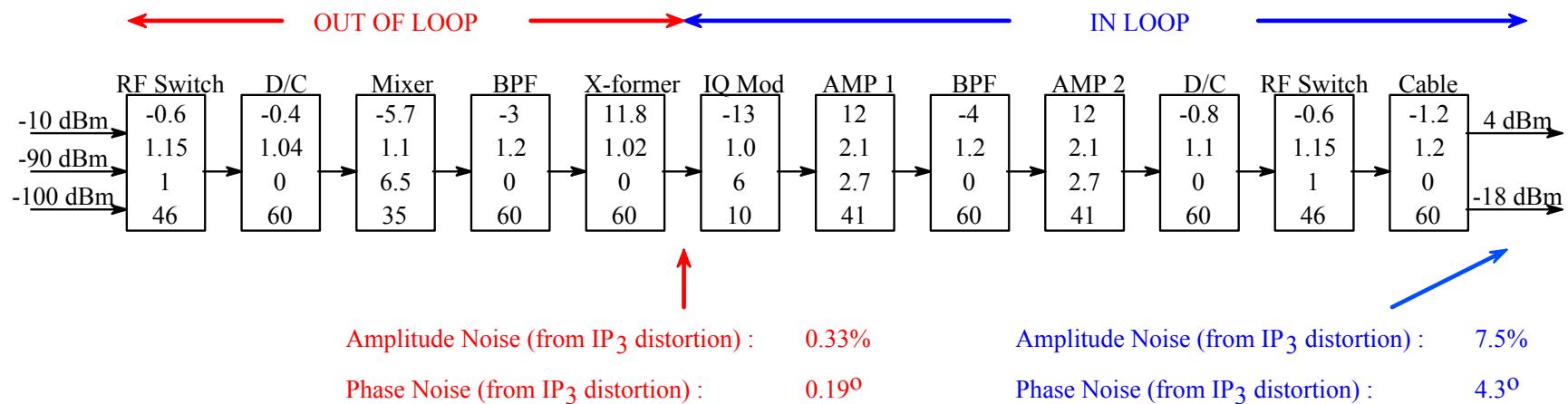
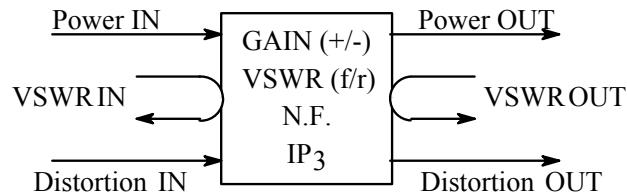
Mother Board Layout



Control Board Layout



Noise Distortion Analysis

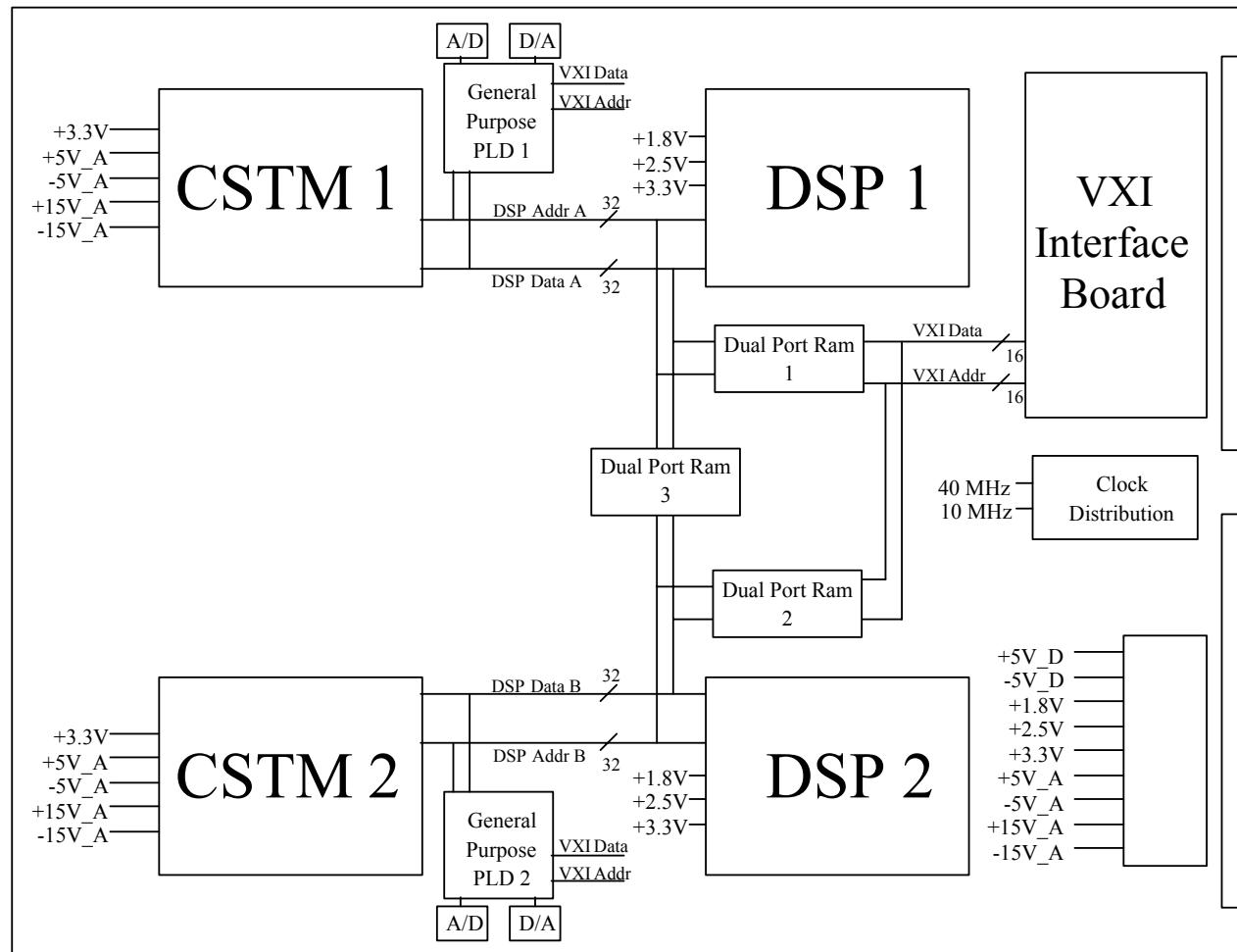


Motherboard Requirements

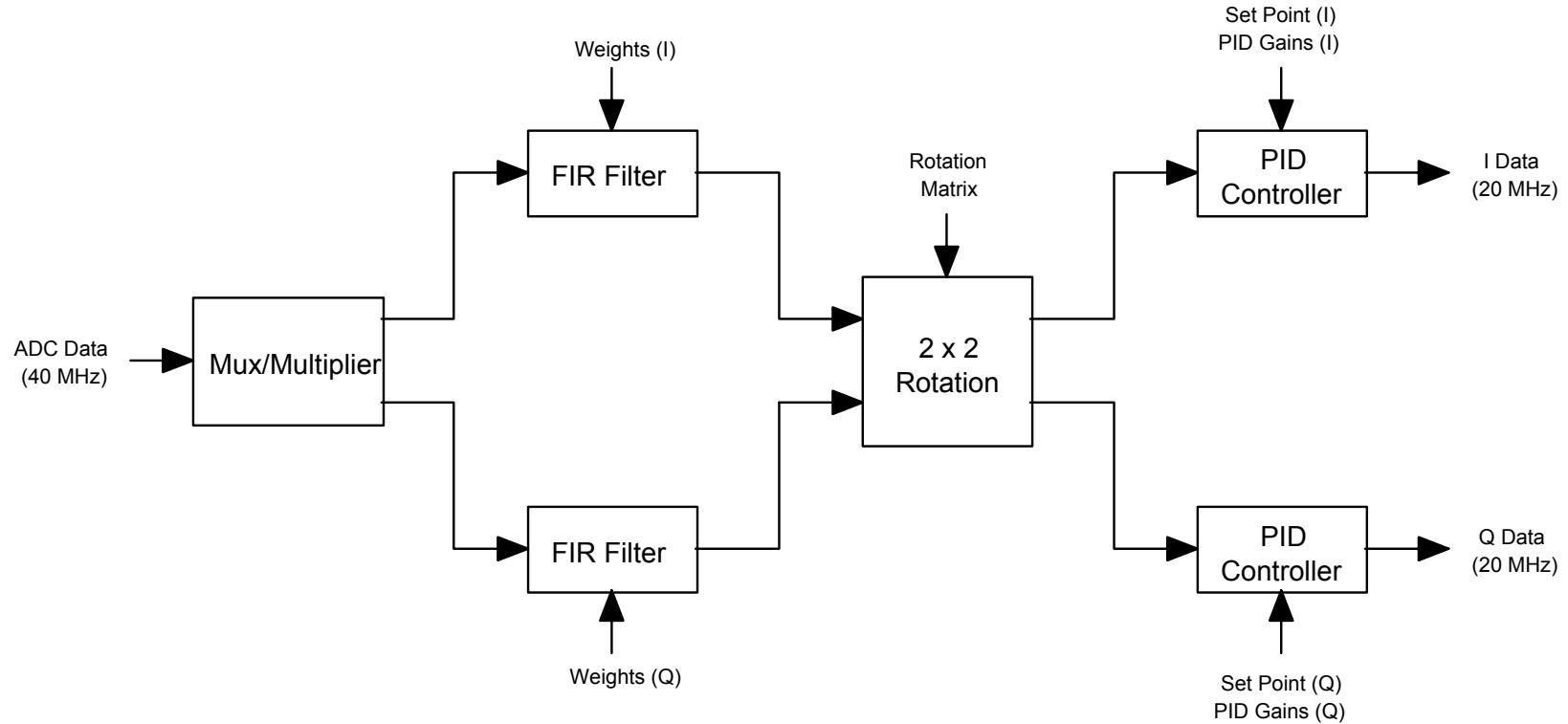


- VXI Interface
- P2 Bus Interface
- Module Interface and Communications
- Clock Distribution
- Power Generation and Distribution
- Diagnostic Circuitry

Motherboard Block Diagram



Fast Signal Processing Architecture



Delay	1	17	1	1	20	cycles
Latency	1.5	1	0	1	3.5	cycles

Fast Signal Processing Timing



- Inherent Filter Delay = 20 cycles (50 ns) = 1000 ns
- Processing Latency = 3.5 cycles (50 ns) = 175 ns
- Total time = 23.5 cycles (50 ns) = 1175 ns

Fast Signal Processing



- Standard PLD Family
 - Altera 20KE Series
 - 672 FineLine BGA Package
 - 20K30E through 20K1500E devices available
 - Cost Estimate
 - EP20K300E - \$460.00 (\$322.00 – 230.00)
 - EP20K600E - \$1740.00 (\$1218.00 – 870.00)



RF Controls Preliminary Design Review

SNS Normal Conducting Linac RF System - Control System Modeling

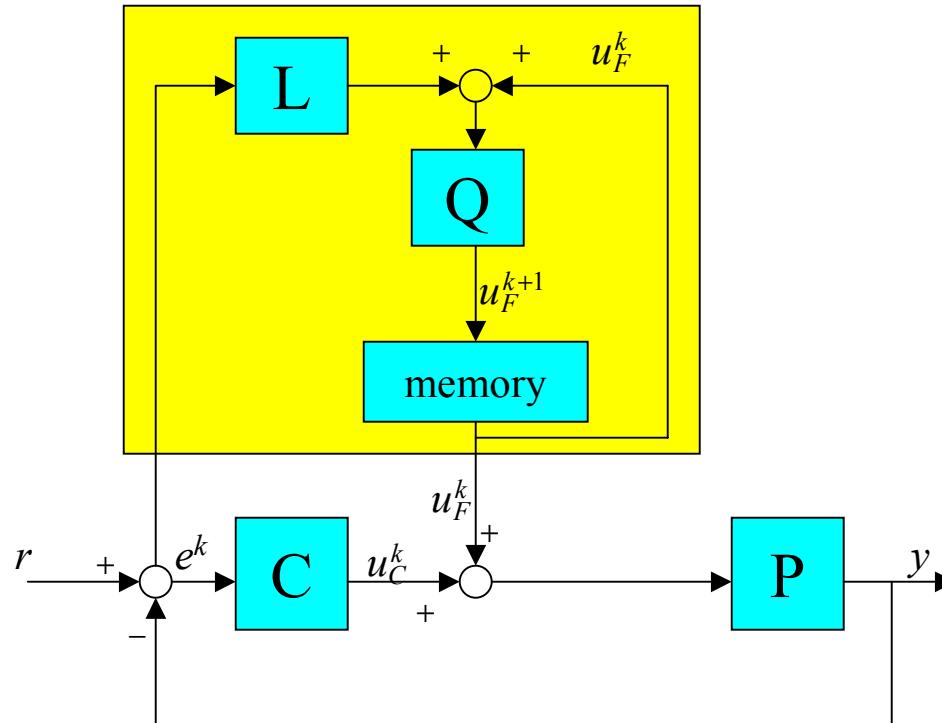
Sung-il Kwon

August 2, 2000

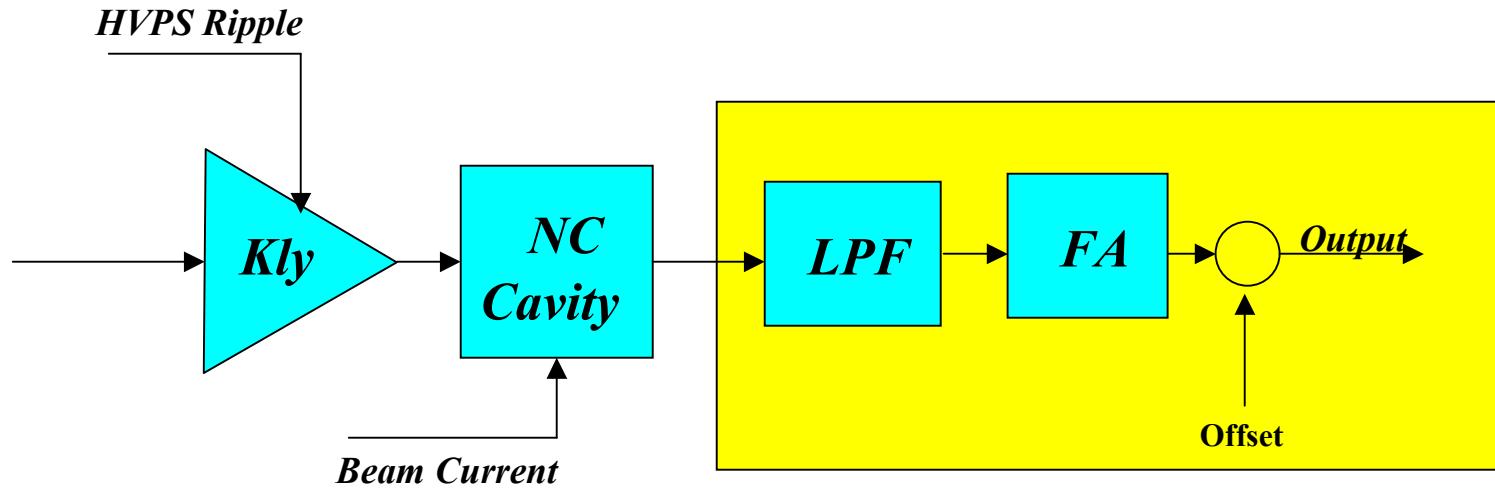
CLOSED LOOP SYSTEM MODELING - PI Controller plus Iterative Learning Controller



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402.5 MHz DTL Open Loop System

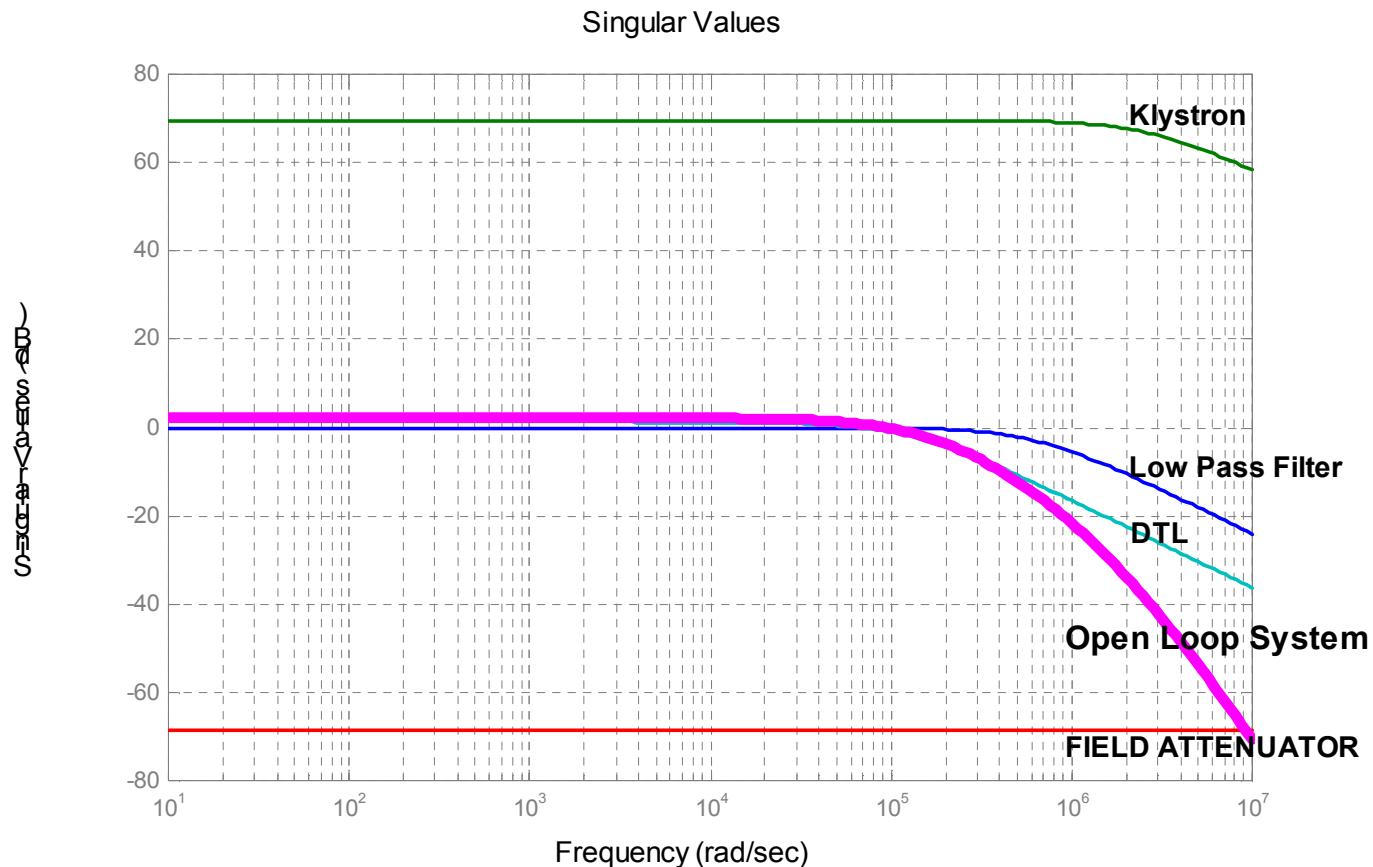


GUI MODELING - Open Loop System



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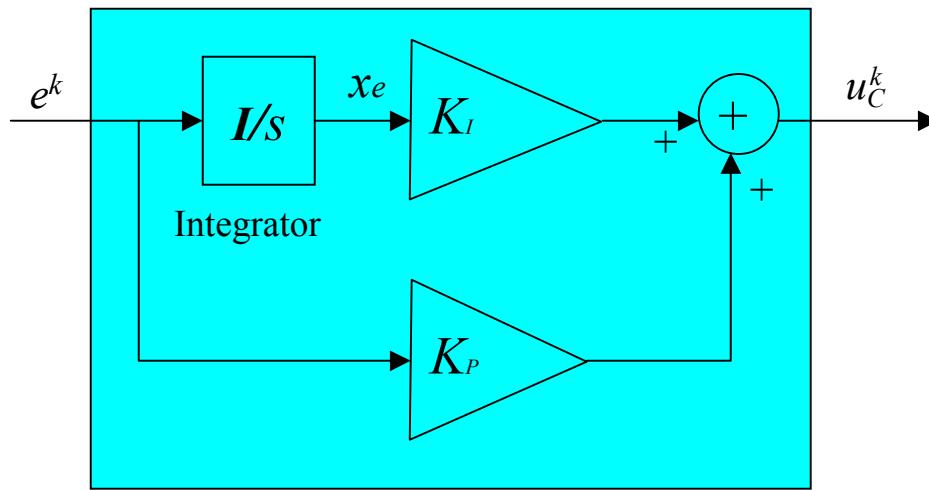
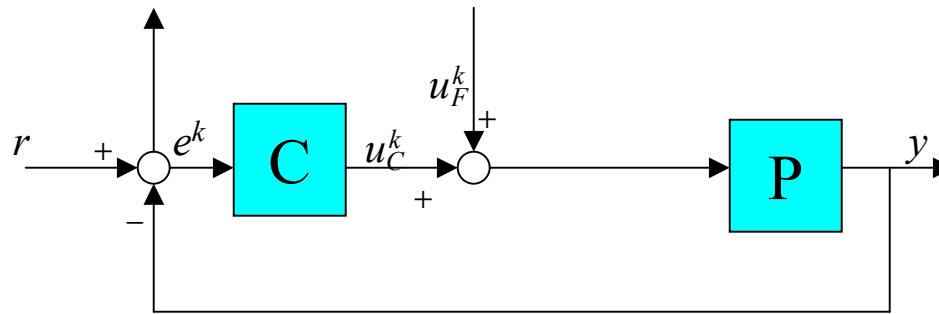
Frequency Responses of the Open Loop System Components



GUI MODELING - PI Controller



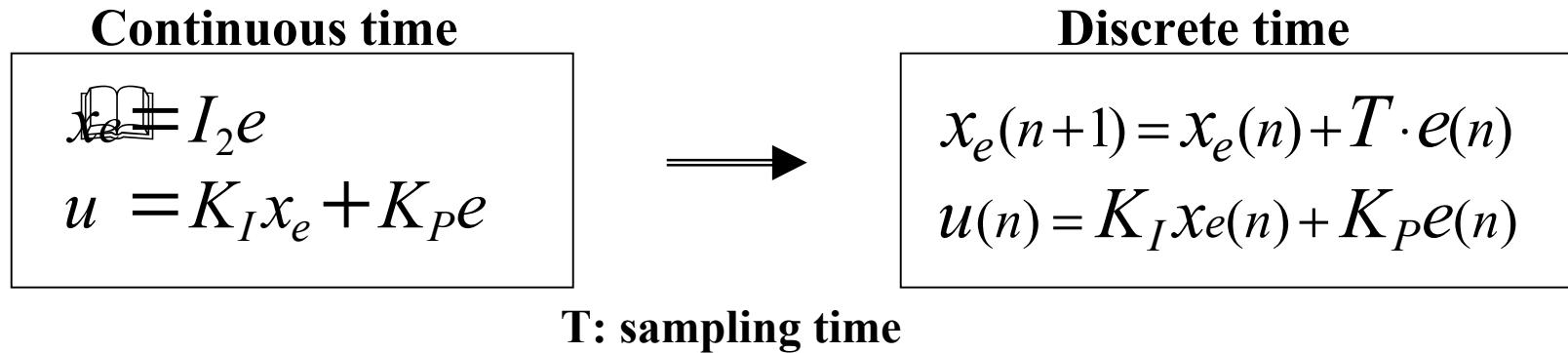
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GUI MODELING - PI Controller

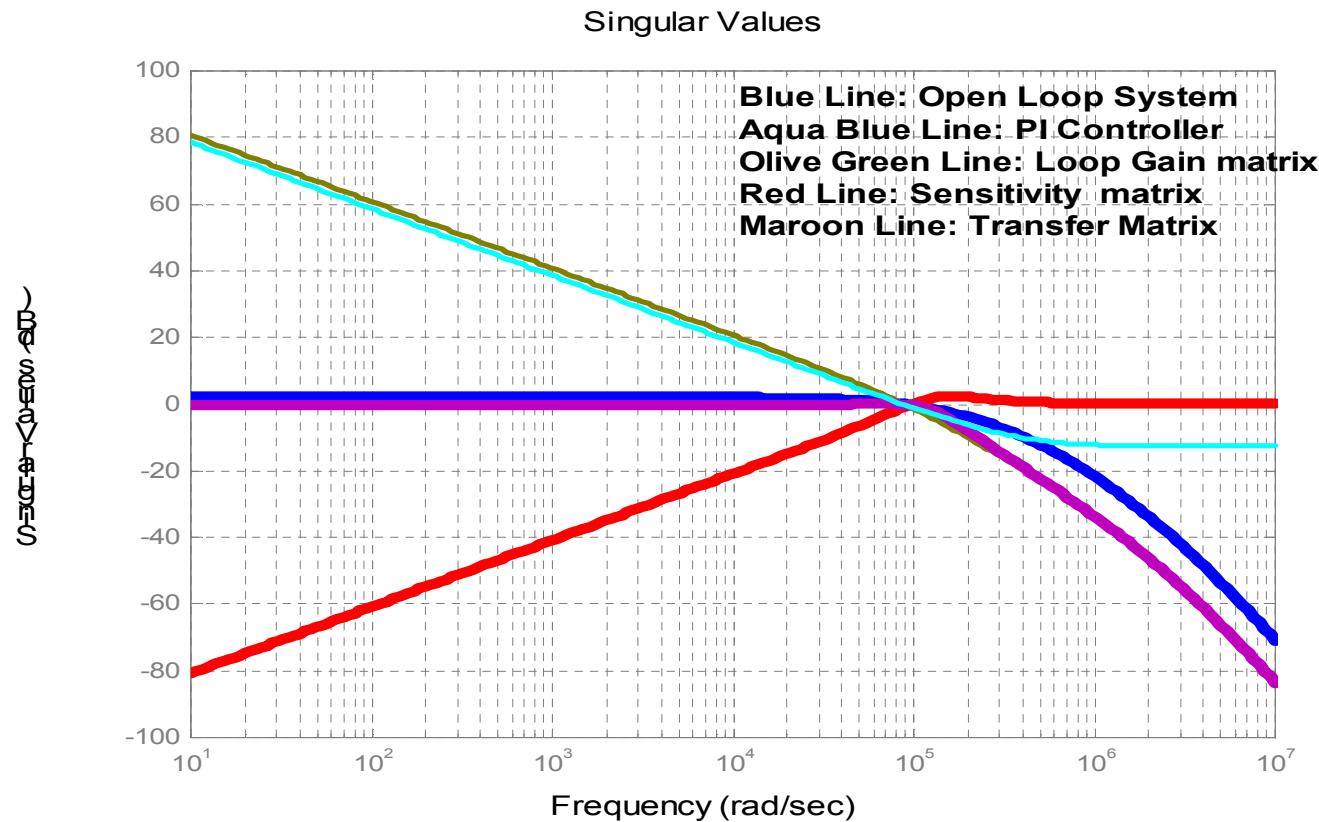


- Outputs
 - PI Controller Gain Matrices K_P and K_I



$$K_I = \begin{bmatrix} k_{I1} & 0 \\ 0 & k_{I2} \end{bmatrix} \quad K_P = \begin{bmatrix} k_{P1} & 0 \\ 0 & k_{P2} \end{bmatrix}$$

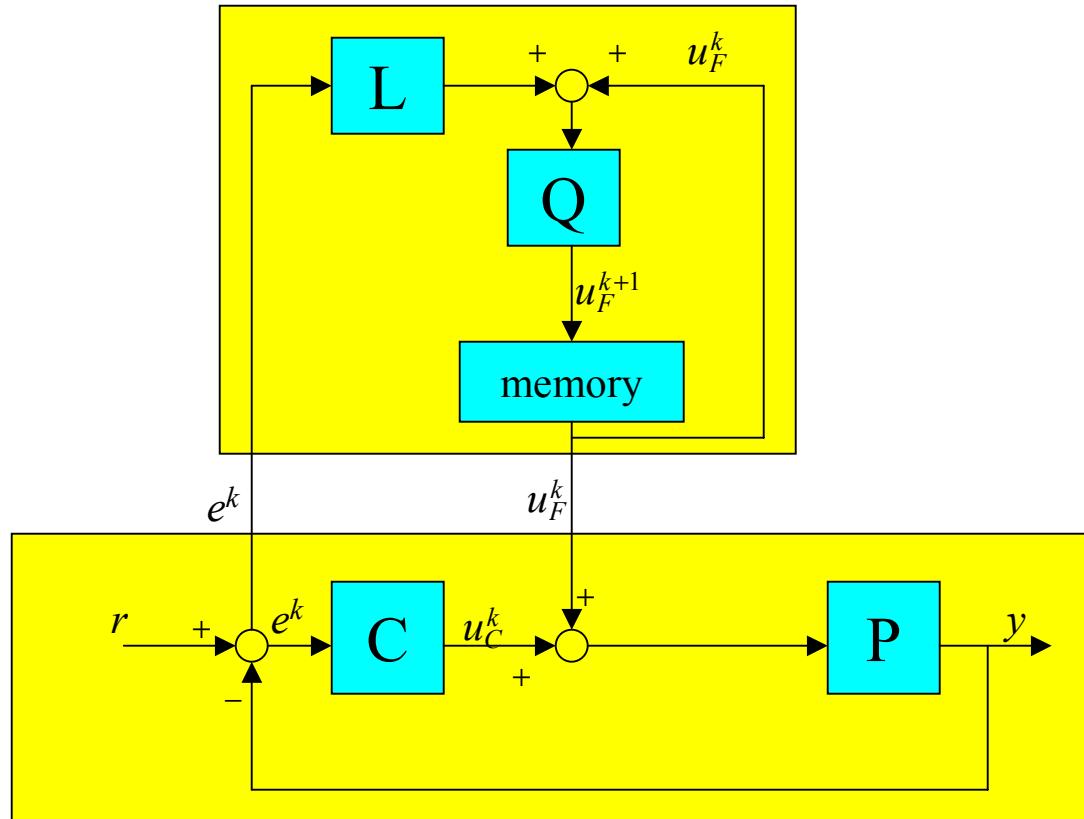
Frequency Response of PI Feedback Control System



GUI MODELING - Iterative Learning Controller (ILC)



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GUI MODELING - Iterative Learning Controller (ILC)



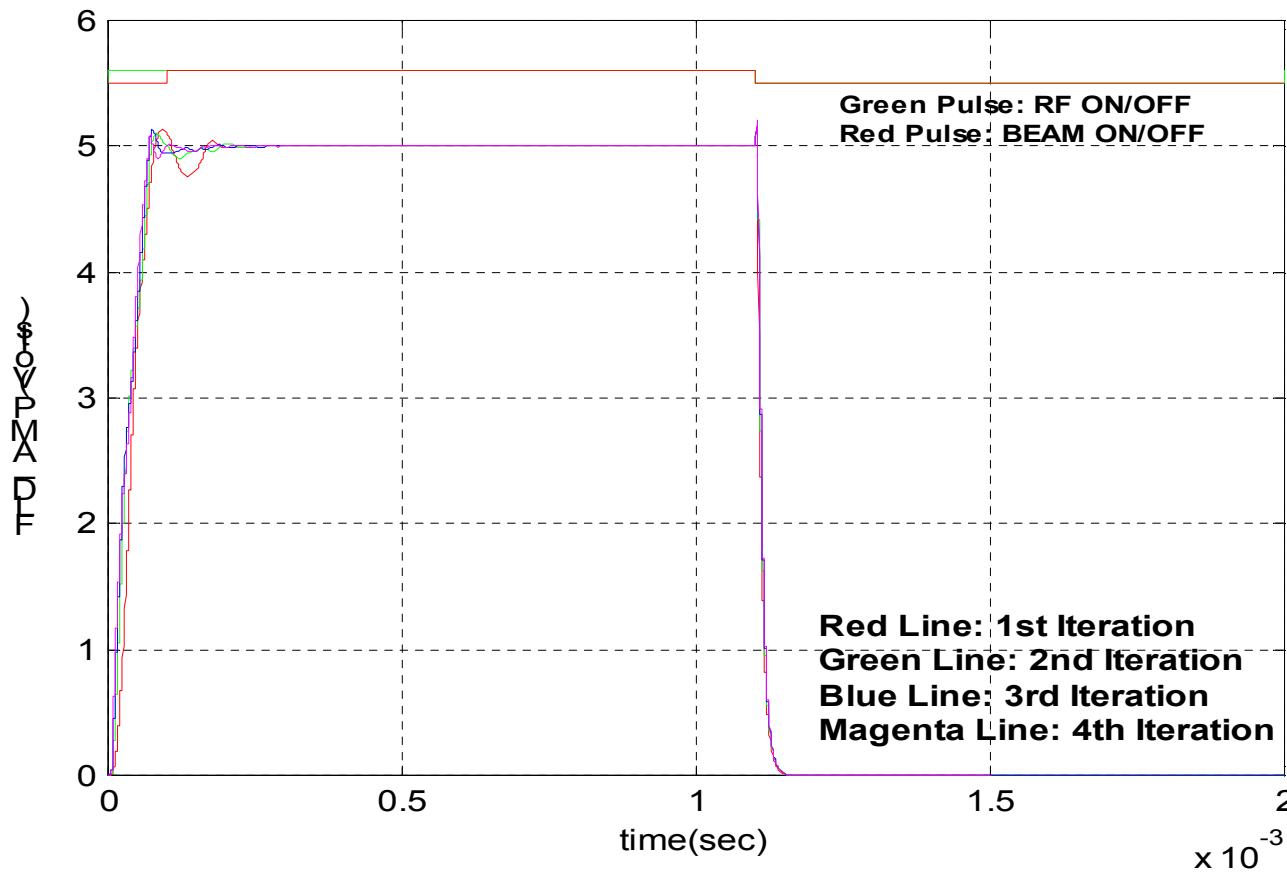
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$$U_F^{k+1} = Q \left(f \cdot U_F^k + \alpha \cdot L E^k \right)$$

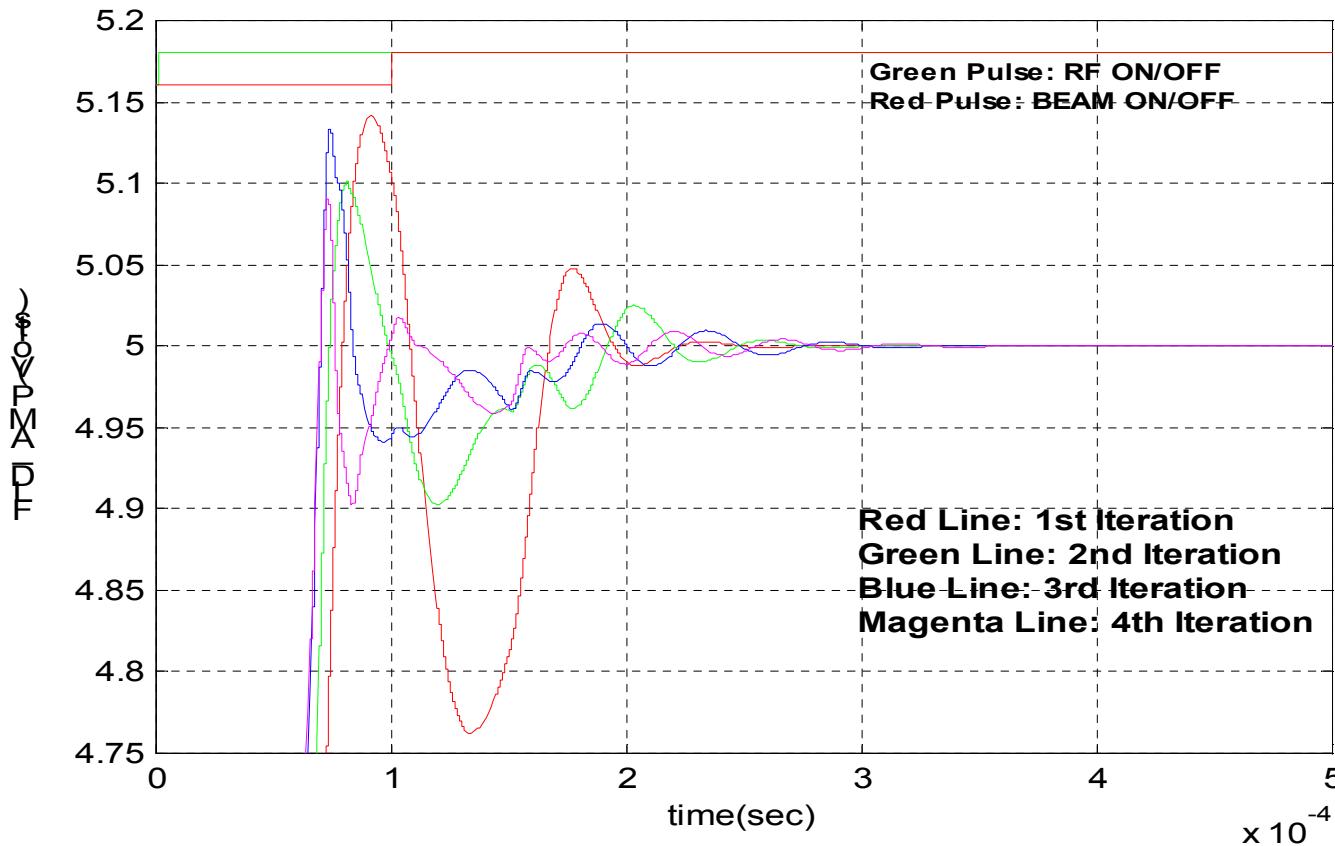
$$\left\| Q \left(f \cdot I - \alpha \cdot L P \cdot (I + C P)^{-1} \right) \right\|_{\infty} < 1$$

$$\lim_{k \rightarrow \infty} E^k = (I + C P)^{-1} R$$

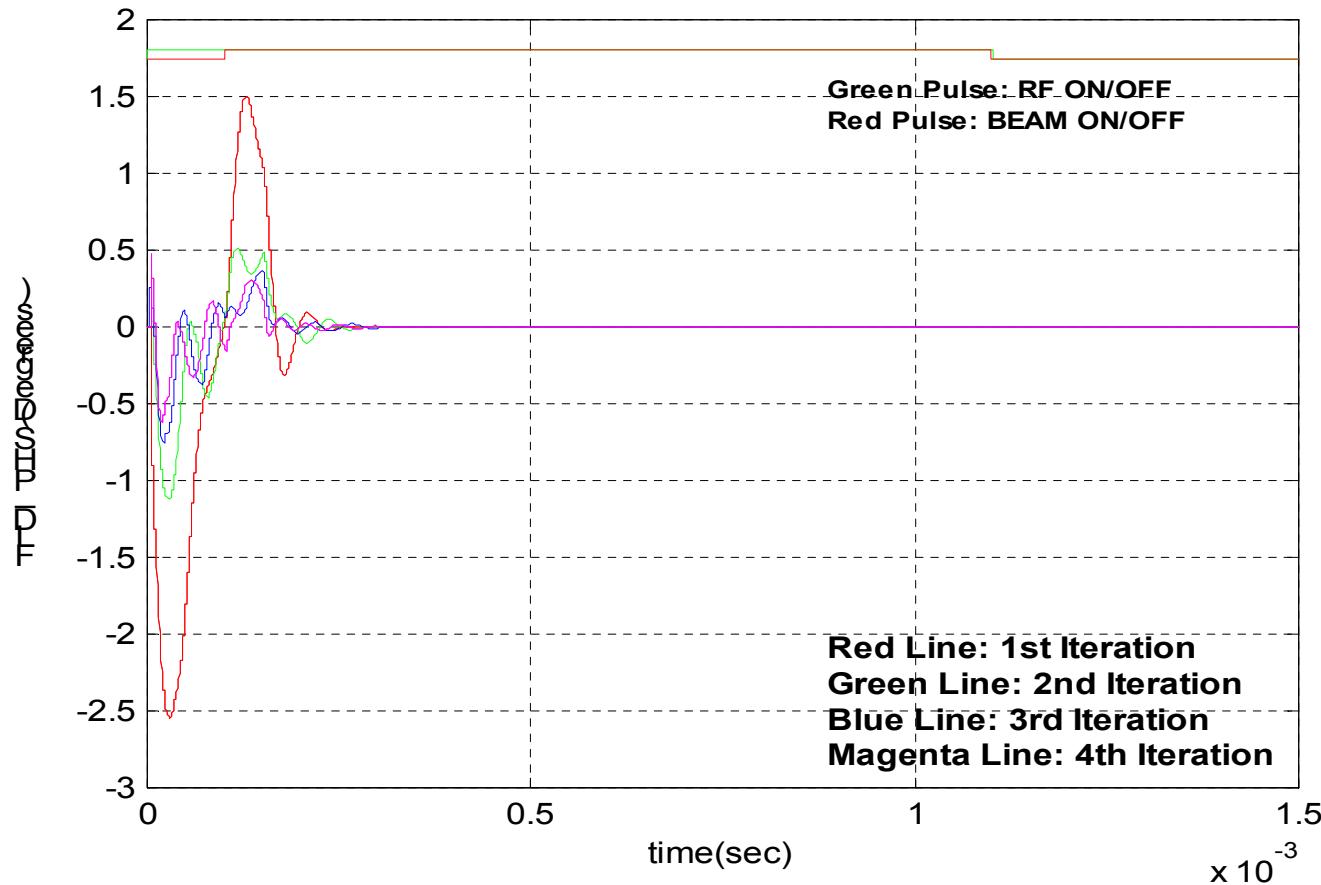
Field Amplitude



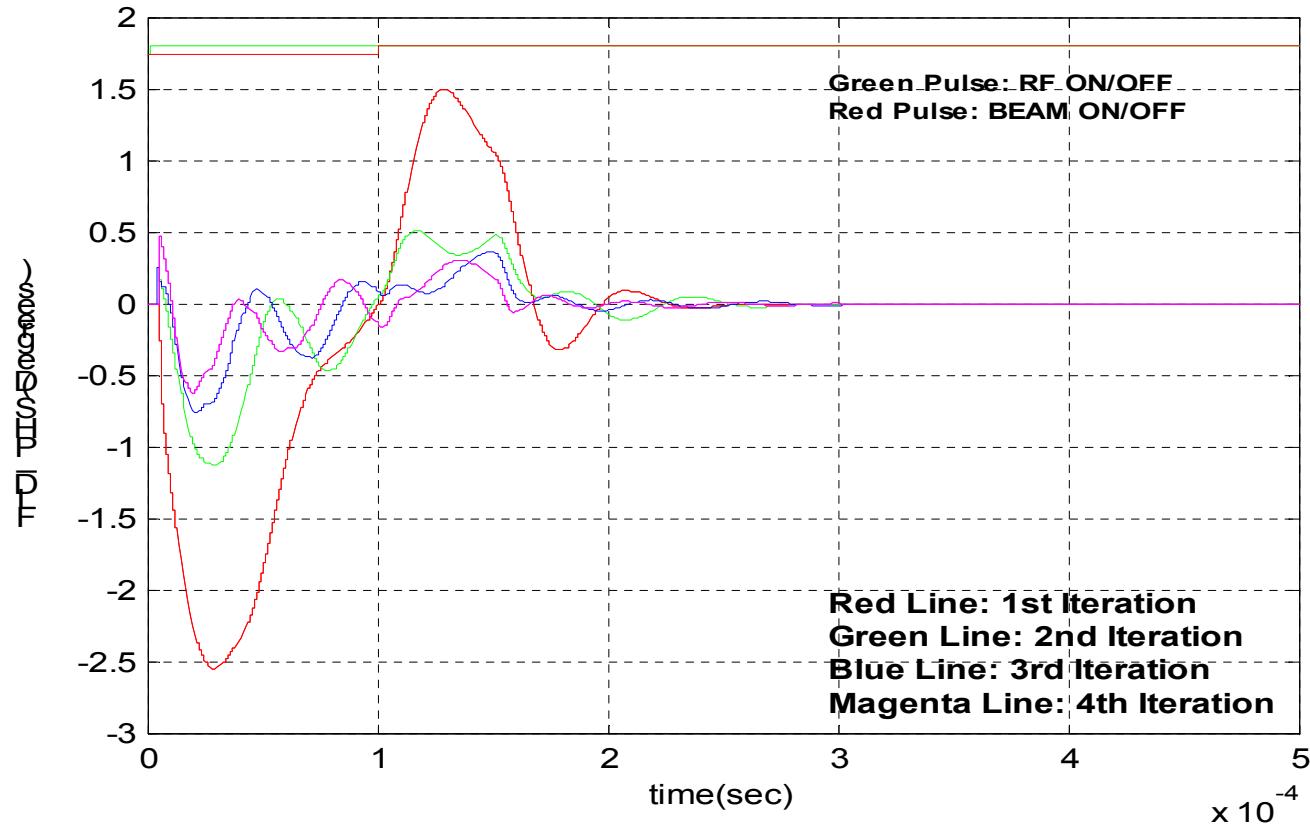
Zoom of Field Amplitude



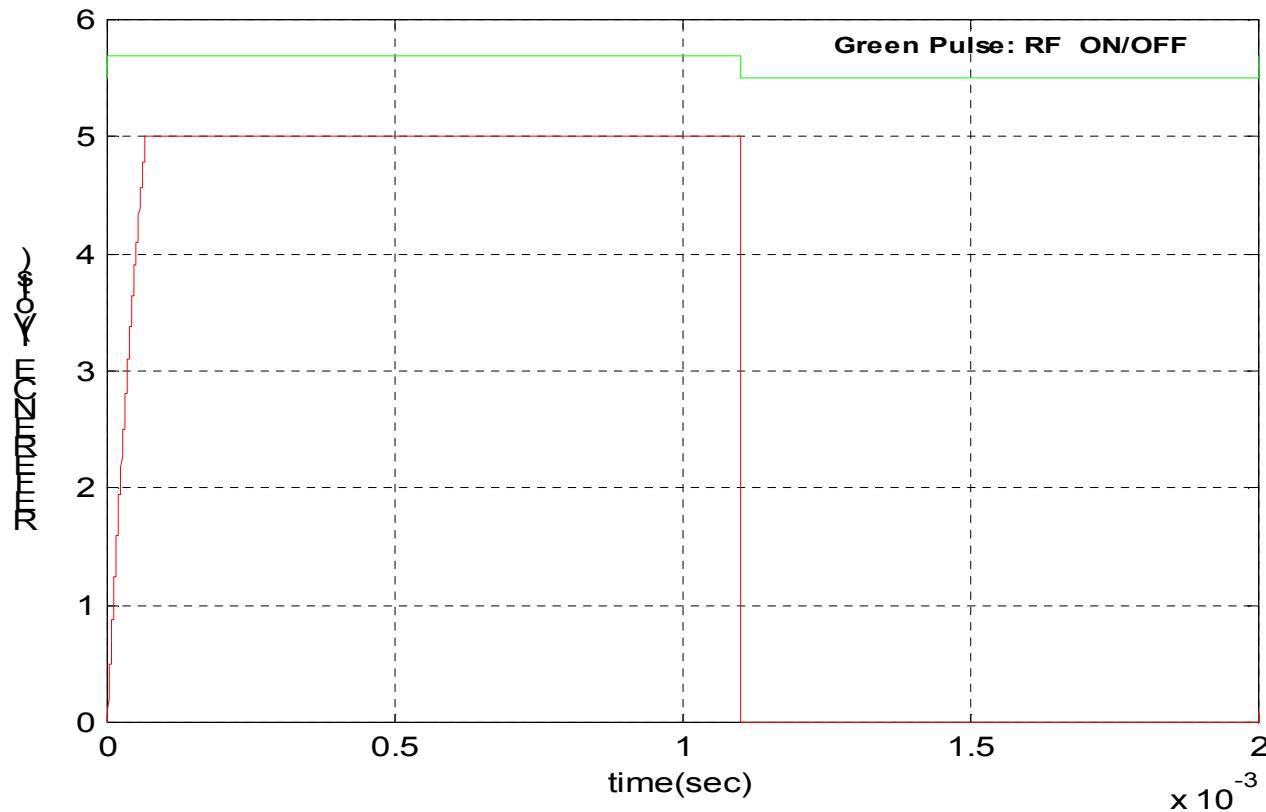
Field Phase



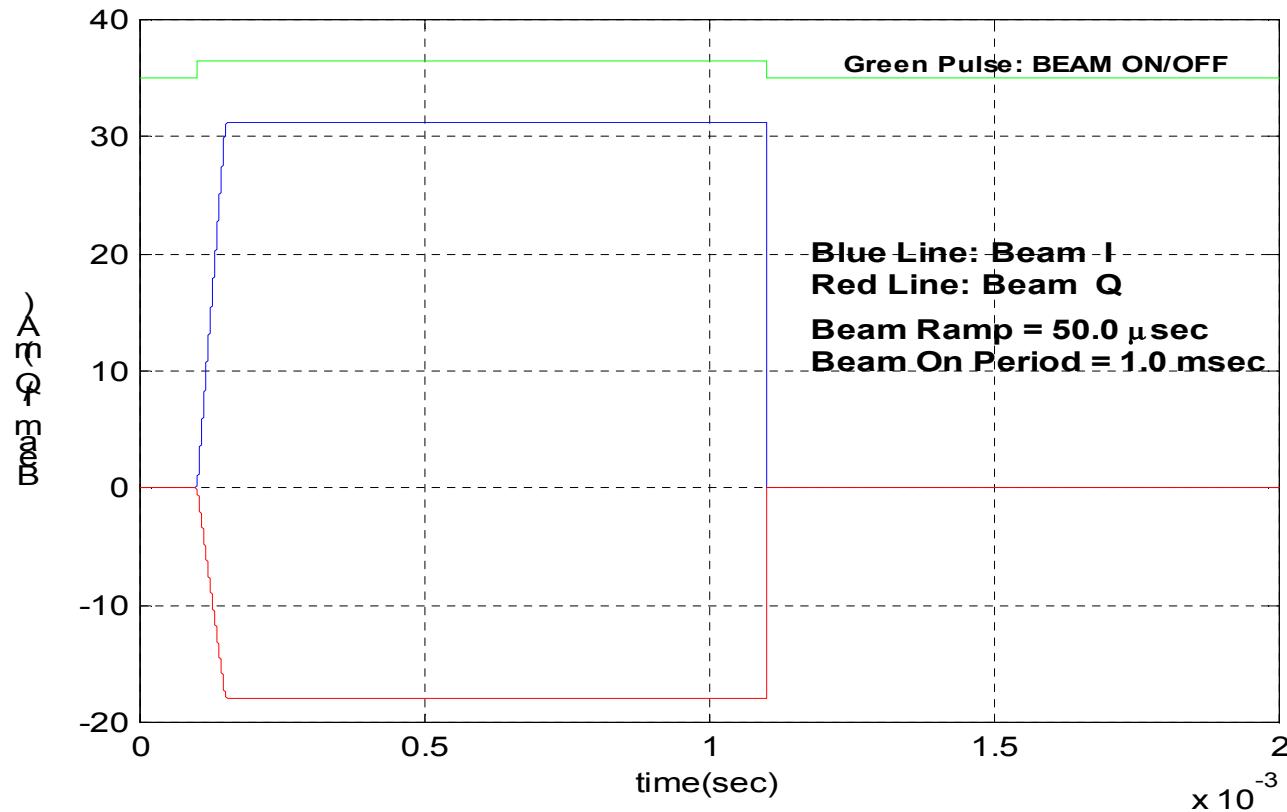
Zoom of Field Phase



Field In-Phase Reference Trajectory



Average BEAM Current Trajectory





RF Controls Preliminary Design Review

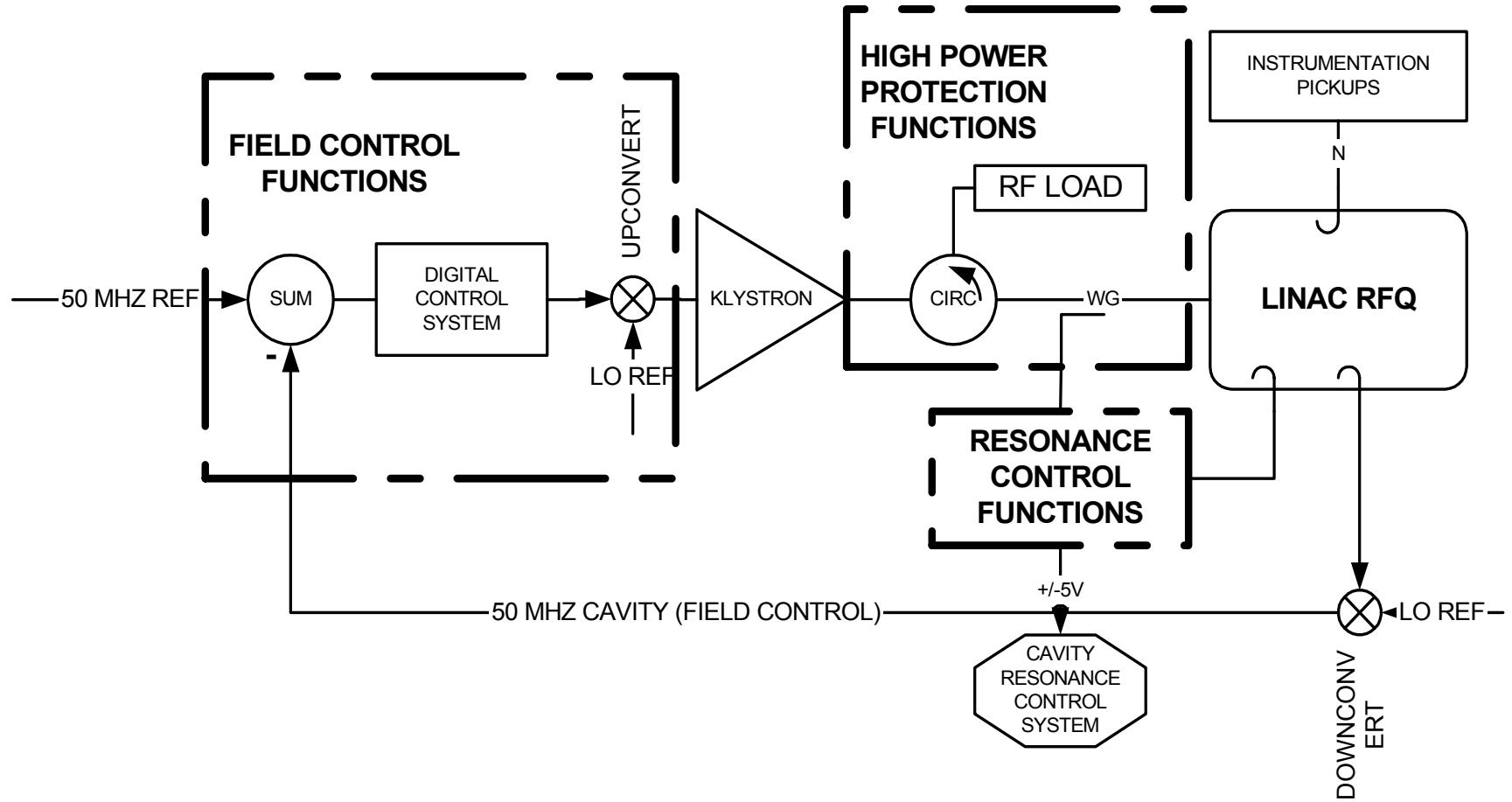
SNS Normal Conducting Linac RF System

High Power Protection Subsystem

Dave Thomson

August 2, 2000

RFCS Functional Block Diagram



HPPS Design Assumptions



- One HPPS module per klystron – no subchassis.
- Limited number of RF channels (6) per module.
- Common FOARC interface (10 channels).
- Same hardware design for all klystrons (NC and SC).
- Cavity arc algorithm will work.
- Protect for two klystrons per crate.
- Vacuum Permit is local input, Fast Protect is global output.
- Fast Protect and Beam Permit *are the same signal* (may be OR'd) to the HPPS.

HPPS Design Requirements



- Monitor waveguide subsystem for RF power faults.
- Monitor Fiber Optic Arc (FOARC) subsystem for arc faults.
- Provide input for Vacuum Permit (local).
- Provide output for Fast Protect/Beam Permit (global).
- Digitize TBD multiplexer channels.
- Simultaneous capture of all RF power levels on a sample pulse from backplane. (One data point per macropulse)

LEDA Lessons Learned 1



- Need to distinguish between cavity arcs and system off resonance in frequency agile mode.
 - Cavity arc → turn off carrier.
 - Off resonance → keep carrier on to heat up cavity.
- Need to identify which klystron faulted and the nature of the fault to the console.
 - Display RF faults (over power condition or cavity arc).
 - Display FOARC faults (which window faulted).
 - Provide FOARC history counters for maintenance.

LEDA Lessons Learned 2



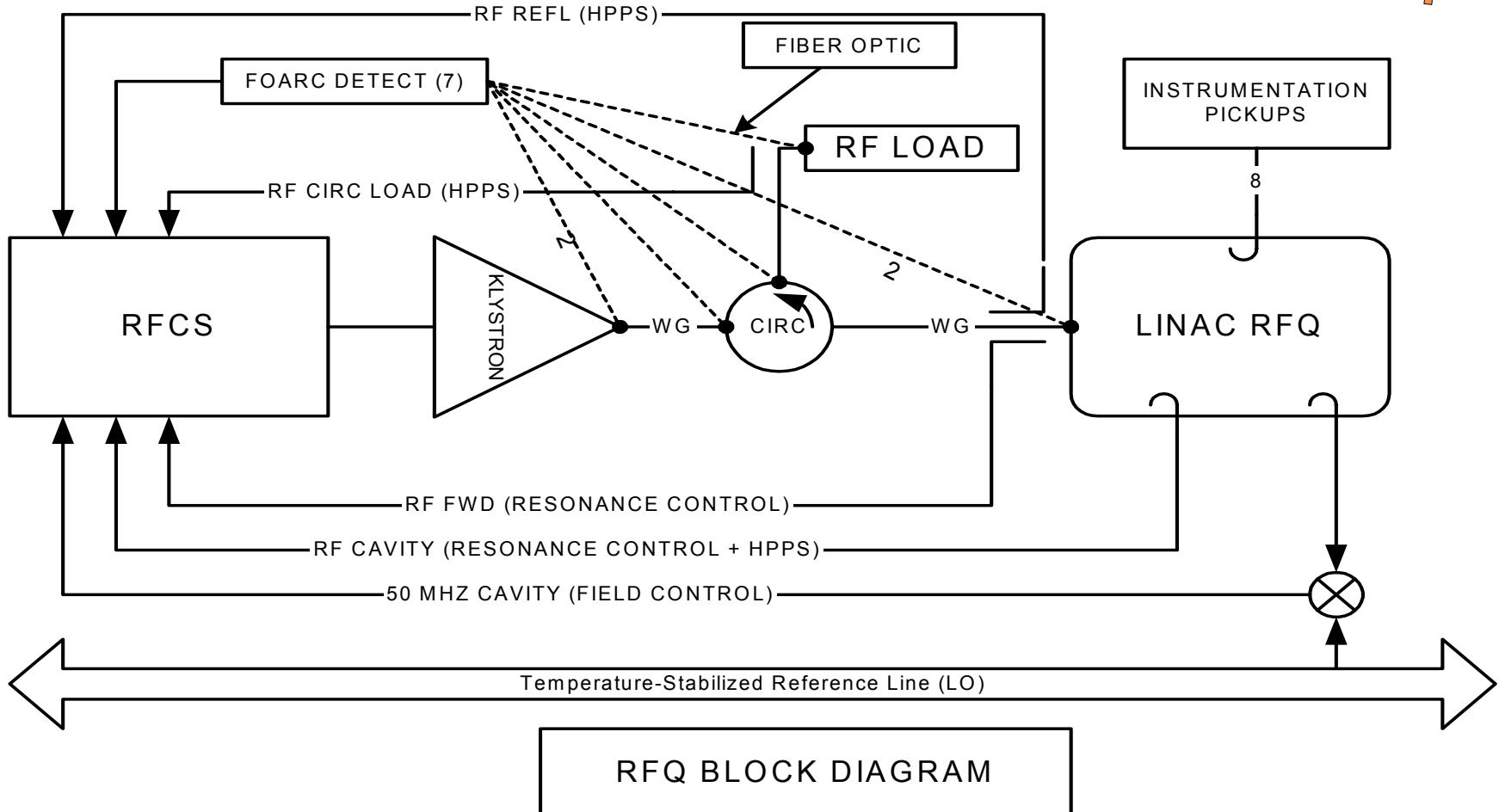
- Minimize analog signal processing with all-digital controls.
- Design for commissioning and maintenance.
 - Minimize the number of operator-settable parameters.
 - Partition the design into logical, testable sub-units.
 - Provide fault isolation/indication with built-in-test and diagnostics.
 - Be able to force the system to a known state to replicate a fault.
 - Need SFMEA (*System Failure Modes and Effects Analysis*) prior to final design freeze to identify fault tree conditions/responses.

LEDA Lessons Learned 3



- EPICS Improvements
 - Need read after write of EPICS parameters.
 - Need reliable EPICS save / reload of configuration files.
 - Selective (klystron by klystron).
 - Major blocks -- e.g.: DTL, CCL, SCRF, HEBT, etc.
 - Need to synchronize the acquisition of the instrumentation channels with the multiplexer.
 - Need safeguards (time over threshold) to keep the operator from killing the RF loads.
 - Need to reduce number of mouse clicks required to dial up parameters. e.g.: use up/down arrows for LSB changes and shift up/down arrows for 10x LSB changes (turbo mode).

Typical RF Block Diagram

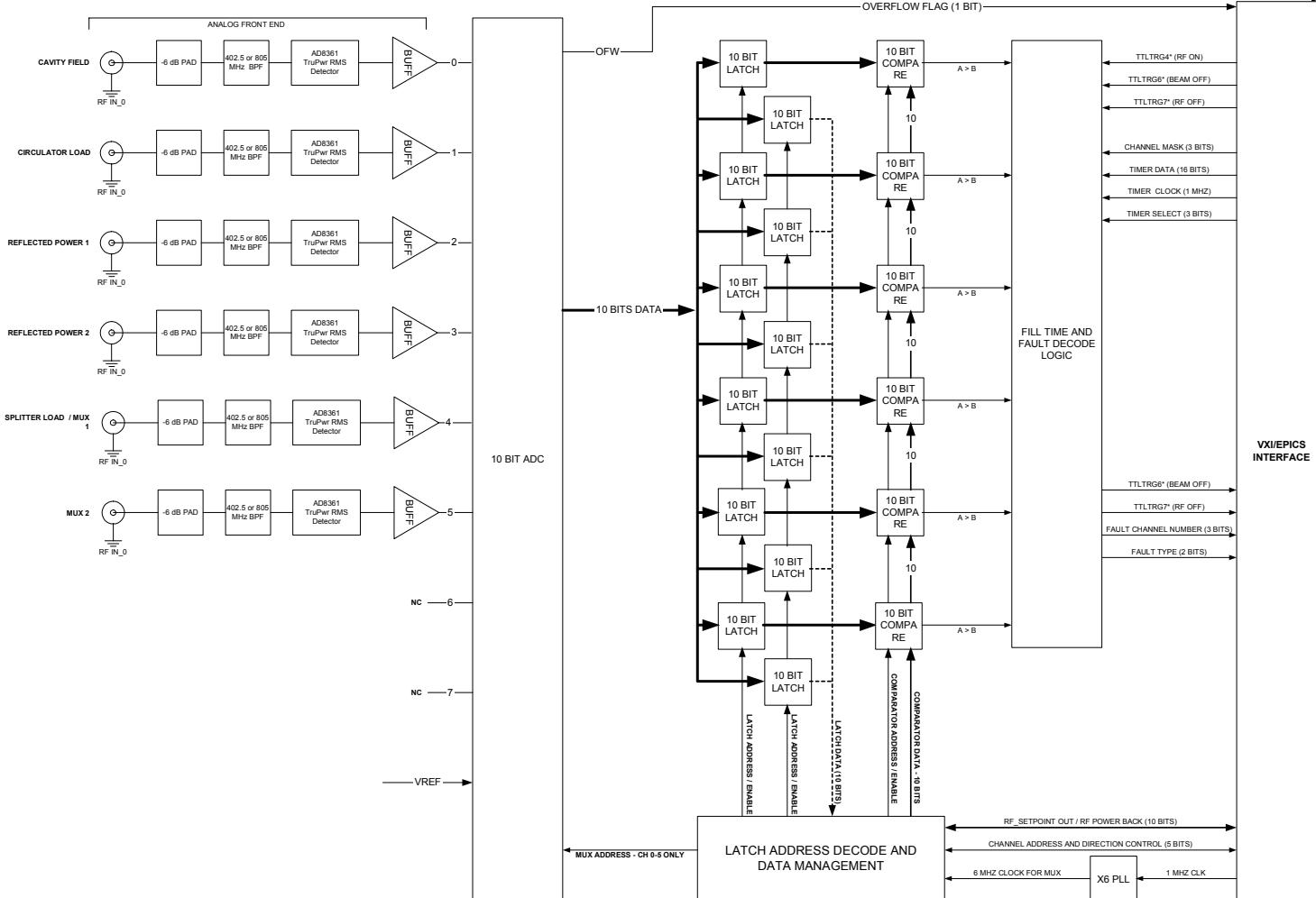


HPPS System Requirements

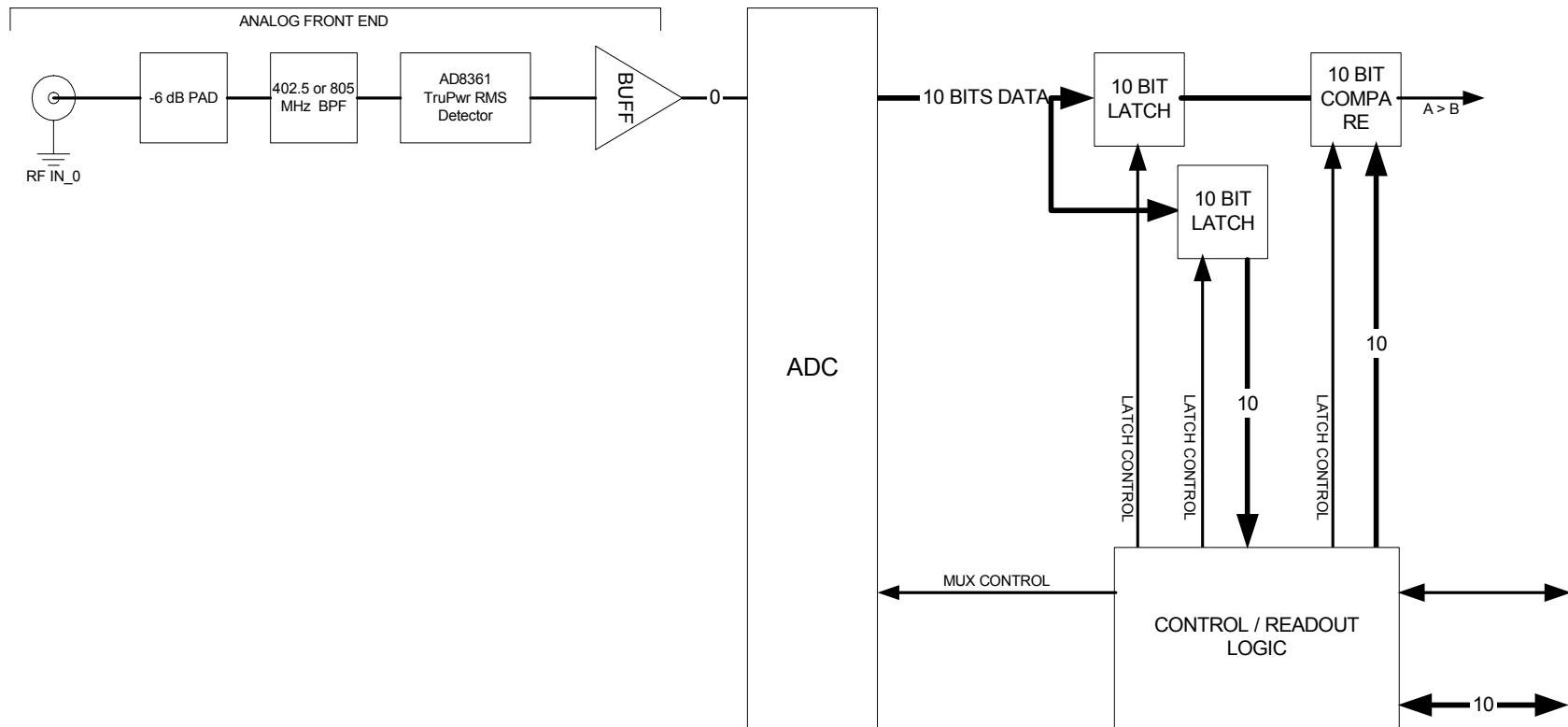


Accelerator Stage	RF Frequency (MHz)	NC RFCS Systems	SRF RFCS Systems	Internal Cavity Field	Cavity Reflected Power	Circulator + Splitter Load	Mux Channels	Total RF Channels per card	Klystron FOARC	Wave-guide FOARC	Total FOARC Channels per card
NC RFQ	402.5	1		1	1	1 + 0	TBD	3	2	5	7
NC DTL	402.5	6		1	1	1 + 0	TBD	3	2	5	7
NC CCL	805	4		1	2	1 + 1	TBD	5	2	8	10
SRF 0.61β	805		33	1	1	1 + 0	TBD	3	2	5	7
SRF 0.81β	805		59	1	1	1 + 0	TBD	3	2	5	7
NC HEBT	805	2		1	1	1 + 0	TBD	3	2	5	7
SNS Systems		13	92								
Test Stand	402.5 & 805	1	1								
Spares	402.5	1									
Spares	805	1	6								
Total RFCS Systems		16	99								

RF Processing Block Diagram



Single RF Channel Example



Signal Processing



- Signal Acquisition
 - 20 MHz BW input filter at 402.5 or 805 MHz.
 - True RMS power detector (AD 8361). No phase info.
 - 6 Ms/s ADC (Zilog XRD 6418 with 6 channels used) with 10 bits resolution.
 - 1 μ s ADC update rate with approximately 2.5 μ s pipeline delay.
 - Digital comparators – no DACs.
 - Total response time $\sim 5 \mu$ s
- PLD Logic decode/actions for speed.
- Parameters set/read via EPICS.

Diode Detector Response



AD 8361 Accuracy



AD 8361 Pulse Response



Fault Maturation Strategy



- Ignore faults during fill time.
- Require faults to persist before they are matured (low pass filter).
- Look at fault frequency (chatter faults).

RF Fault Actions



- Blank RF carrier (TTLTRG7*) to end of macropulse if:
 - Power is over threshold on splitter or circulator load.
 - Power is over threshold on cavity reflected power (but see also frequency agile mode).
 - Cavity arc is detected.
 - FOARC is detected.
 - Vacuum permit faults.
- Blank **BP/FP** (TTLTRG6*) to end of macropulse if TTLTRG7* chatter faults (too many macropulse RF blanks in a row). Frequency is an EPICS settable parameter.
- Both RF & FP remain blanked as long as fault persists.

RF Cavity Arc Detection Strategy



- *IF* (RF is enabled) *AND* (cavity power is below threshold) *AFTER* (FILL_TIME expires) *THEN* (declare an ARC_FAULT and blank TTLTRG7* to the end of the macropulse).
- Should work for both NC and SC cavities.
- Proposed by Lloyd Young based on LEDA experience.
- **OR:** *IF* (high reflected cavity power) *AND* (cavity power below threshold) *AFTER* (FILL_TIME expires) *THEN* (declare an ARC_FAULT and blank TTLTRG7* to the end of the macropulse).
- Need to define frequency-agile mode off-resonance actions.

Waveguide Arc Detection Strategy



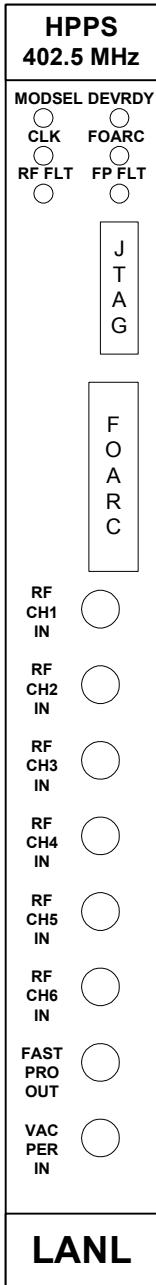
- Waveguide arcs are detected by the High Power RF group using fiber optic transducers (FOARCs) and signaled to HPPS *via* opto-isolated TTL control lines.
- Any FOARC blanks the carrier (TTLTRG7*) to the end of the macropulse. The channel which arced is displayed by EPICS.
- FOARCs are logged to 16 bit history counters for long-term diagnostic purposes and read/reset manually *via* EPICS.

Inputs/Outputs



- Six RF channel inputs with true RMS detection.
- Ten opto-isolated FOARC inputs with single LED display.
- One opto-isolated vacuum permit input (local cavity vacuum).
- **Fast Protect** output (*aka Beam Permit or TTLTRG6**) with front panel LED. Assumption is that **FP** = **BP** at this level.
Actual FP/BP Interface to SNS control system is TBD.
- RF Fault backplane output (TTLTRG7*) with front panel LED.
- Clocks and sample pulse received off backplane for synchronization with rest of system.
- Adjustable parameters set and read back *via* EPICS.

Front Panel Concept



Built-in Test / Diagnostics



- Provides “Lamp test” for FOARC inputs. Can set FOARC line in Klystron rack from HPPS *via* EPICS.
- HPPS provides “Who faulted” signal *via* EPICS for TTLTRG6* and TTLTRG7*.
- Counters for FOARC history (one 16 bit counter per channel).
- LEDs for MODSEL, DEVRDY, CLK, FOARC, RF FAULT and FP FAULT on front panel.
- Firmware reflash *via* JTAG on front panel.
- EPICS read back of all software-settable parameters.
- Reduced complexity compared to LEDA system should improve reliability.

Newly-discovered Requirements



Questions / Action Item Review



- How many RF mux channels for each segment? Do we need a dedicated mux digitizer card?
- Does HPPS need to monitor or respond to Fast Protect and/or Beam Permit input to turn off RF? Are they the same? What is interface to the rest of the control system?
- Does HPPS need an RF injection signal for built-in-test?
 - Could use existing RF signals in the crate, but would require manual plug/unplug to set up.
- Need to define EPICS interface and variable names.
- Need to define frequency-agile (off-resonance) mode RF fault management strategy.



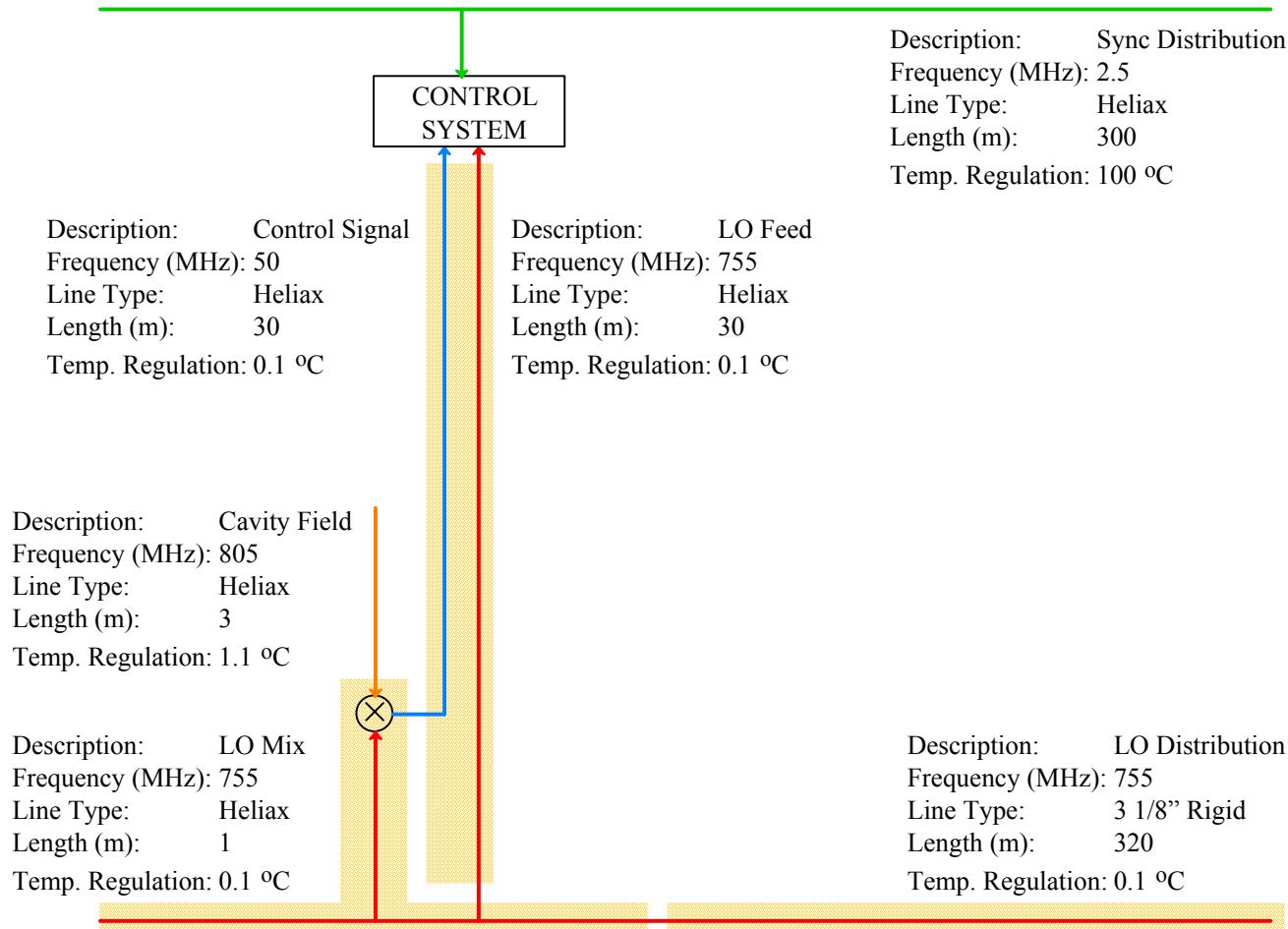
RF Controls Preliminary Design Review

SNS Frequency Distribution

Tony Rohlev

August 2, 2000

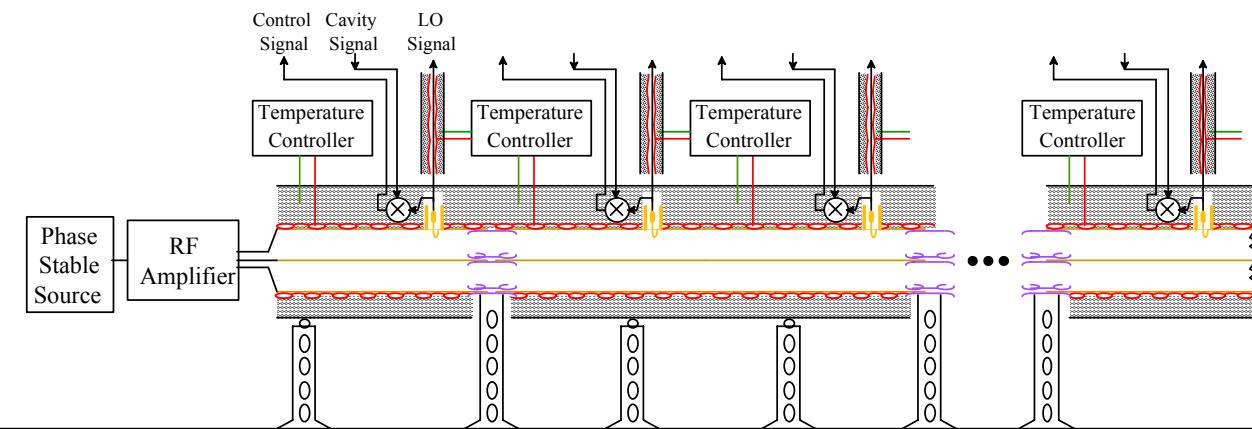
SNS Frequency Distribution Criteria



SNS Reference Line Specifications



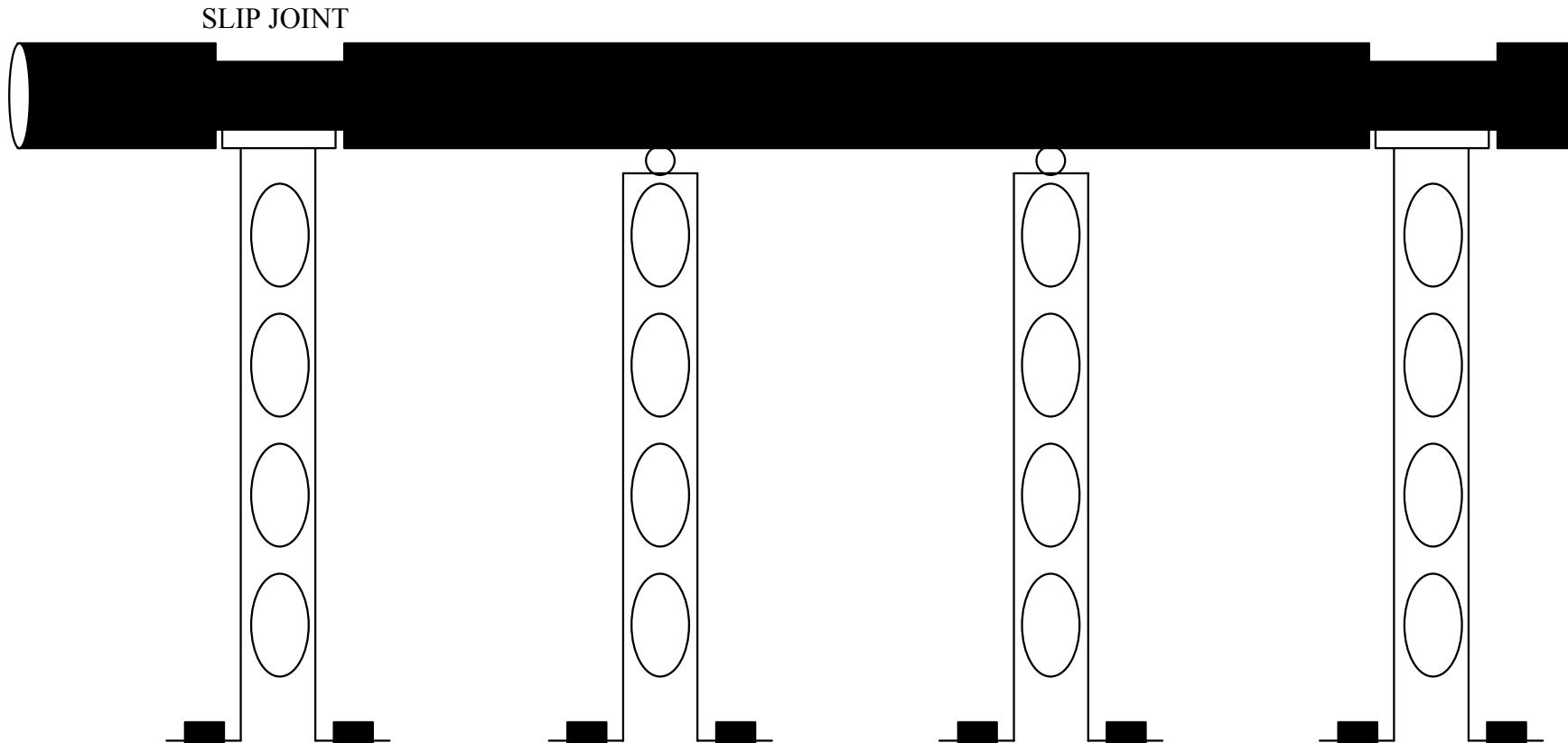
Frequency:	755 MHz
Length:	320 m
Phase Stability:	0.1° @ 755 MHz
Number of Taps:	95
Tap Power:	21 dBm
Tap Coupling:	> 20 dB, variable in 1 dB steps
Amplifier Power:	50 Watts
Line Type:	3 1/8" rigid copper co-ax; pressurized with dry Nitrogen
Line Lengths:	20 ft. sections with slip joints every 100 ft.
Temperature Control Method:	Electric heater and controller every 100 ft.
Temperature Control:	0.1 °C (40 °C nominal temperature)
Pressure Control:	+/- 1 torr
Line Type:	3/8" Heliax for LO distribution to Clock Module
Line Lengths:	100 ft. insulated and temperature controlled to 0.1 °C @ 40 °C.



SNS Reference Line



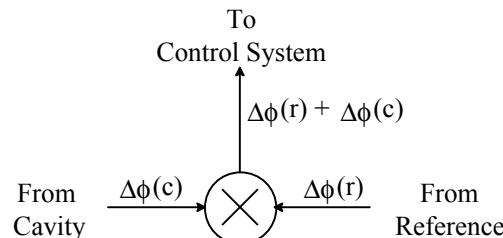
Pipe Diameter: 12 in
Post to Post Spacing: 33 ft
Pipe Weight: 5 lb/ft



Terms Definitions and Values



- At 755 MHz: $\lambda = 40 \text{ cm} @ c$
 $0.1^\circ \text{ (electrical } @ c) = 110 \mu\text{m}$
- 3 1/8" co-ax: Rigid copper pipe (both inner and outer) Teflon supports for inner conductor
Propagation velocity = 0.998 c
Thermal expansion = 16.6 ppm/ $^\circ\text{C}$
Loss: 0.942 dB/100m @ 755 MHz
Electrical phase change in 100 ft section for 1 $^\circ\text{C}$ temperature change = 0.46 $^\circ$ @ 755 MHz
Andrew part number: 562A
- 3/8" co-ax: Flexible copper co-ax, foam filled
Propagation velocity = 0.88 c
Thermal expansion = 5.6 ppm/ $^\circ\text{C}$
Loss: 0.52 dB/100m @ 2.5 MHz
2.46 dB/100m @ 50 MHz
9.96 dB/100m @ 755 MHz
Electrical phase change in 100 ft section for 1 $^\circ\text{C}$ temperature change = 0.18 $^\circ$ @ 755 MHz
Electrical phase change in 100 ft section for 1 $^\circ\text{C}$ temperature change = 0.01 $^\circ$ @ 50 MHz
Electrical phase change in 1000 ft section for 102 $^\circ\text{C}$ temperature change = 180 $^\circ$ @ 755 MHz
Andrew part number: LDF2-50



Clock Module Overview



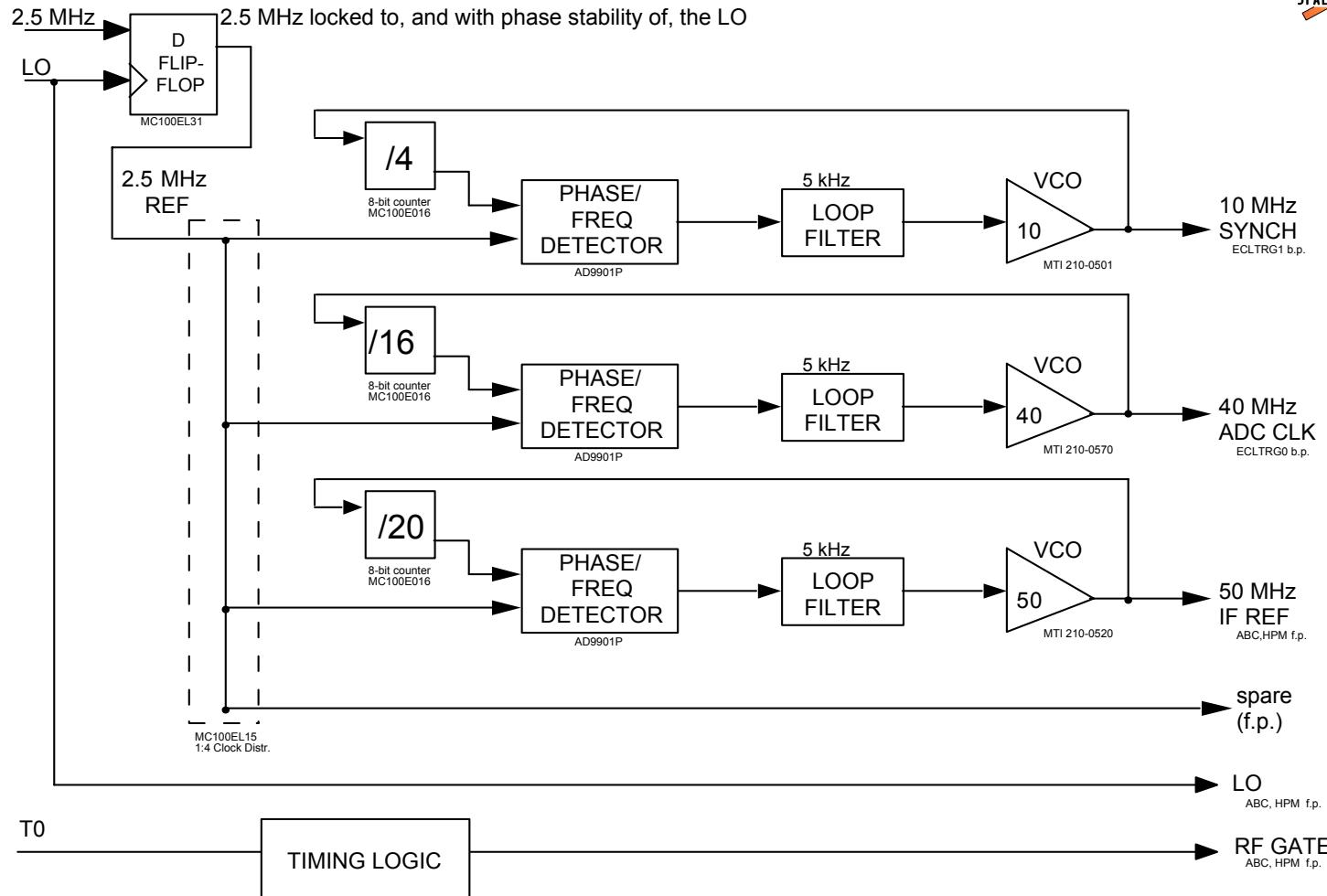
- REQUIREMENTS AND SPECIFICATIONS
- CDM WITHIN OVERALL RF CONTROL SYSTEM
- BLOCK DIAGRAM
- I/O REQUIREMENTS
- FAILURE/RESET MODES
 - BUILT IN SELF-TEST

REQUIREMENTS & SPECIFICATIONS

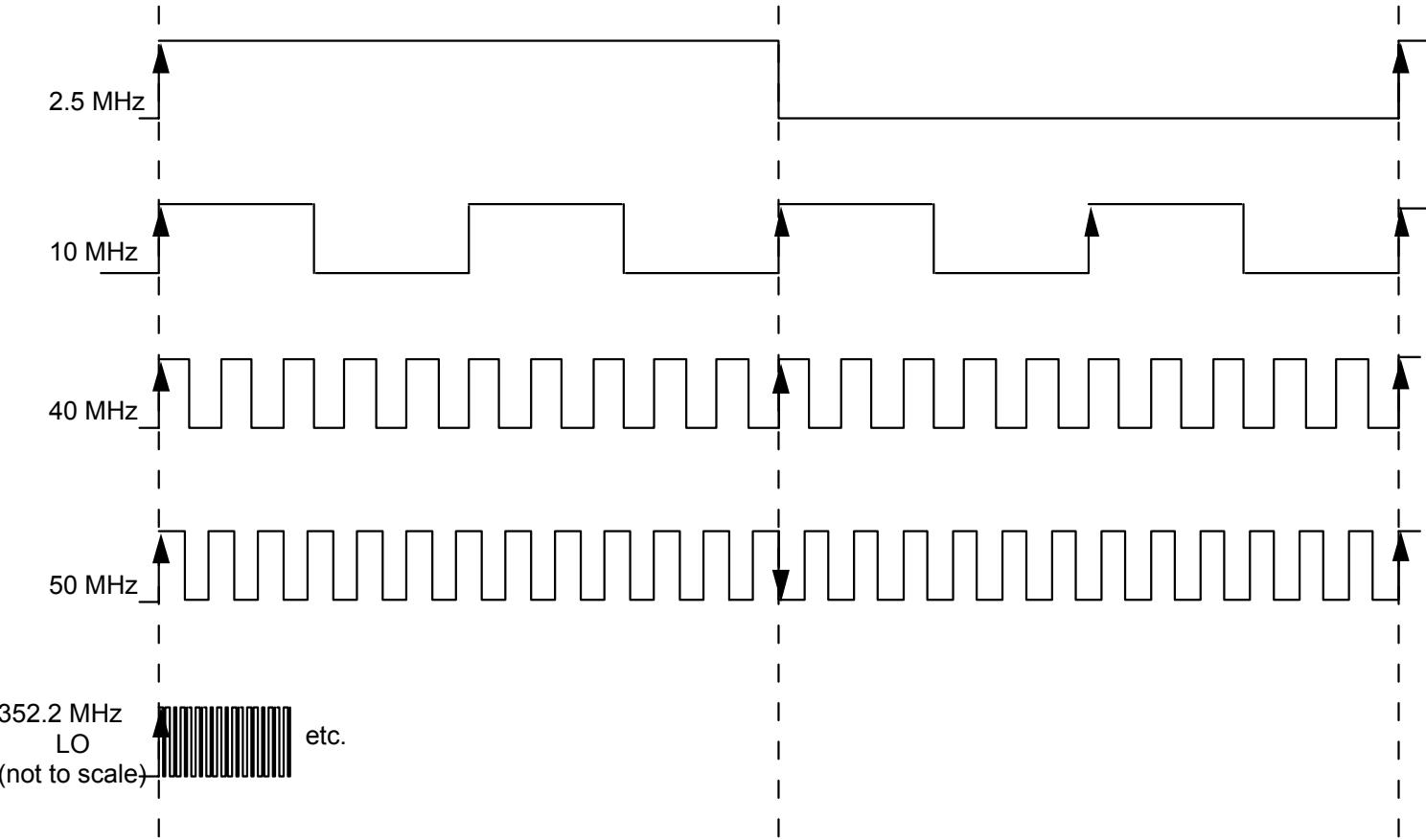


- PROVIDE SYNCHRONIZED CLOCKS TO ALL RF CONTROL MODULES.
 - ALL DERIVED FROM, & PHASE-LOCKED TO, THE MASTER OSCILLATOR
- PHASE-LOCKED OUTPUTS:
 - 40 MHz ADC CLOCK (± 0.1 degree)
 - 50 MHz IF (± 0.1 degree)
 - 352.2 (755) MHz LO (± 0.1 degree)
- OTHER OUTPUTS (backplane)
 - SYNCHRONIZATION PULSE (10 MHz)
 - RF GATE
 - SAMPLE
- INPUTS
 - 2.5 MHz REFERENCE
 - LO (temperature compensated)
 - TIMING (front panel)

Clock Module Phase-Locked Loop Implementation



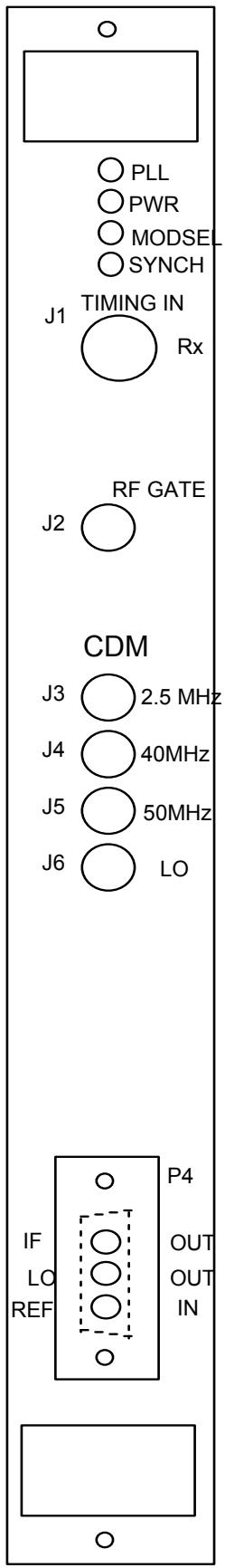
Clock Module Timing Relationships



Clock Module Front Panel



SPALLATION NEUTRON SOURCE



CDM STATUS/SUMMARY



- MODULE WILL PROVIDE SYNCHRONIZED CLOCKS
- 40, 50 MHz LOOPS HAVE BEEN BREADBOARDED
- FAULT CIRCUITRY BUILT AND TESTED
- STILL NEED TO TEST STABILITY OF LOCKING THE 2.5 MHz TO THE STABLE LO
- SCHEMATICS PARTIALLY COMPLETE IN ORCAD
- WHAT HAVE I MISSED?

Manufacturing Plan

Irene DeBaca



Fabrication & Testing RF Control System

Prototype Designs & Temp-Cycle
(in house)

- Specifications
- Capabilities Required
- Resources

Specifications

100% Inspection
IPC 610 CLASS 3

Resources

Sparton
Delta Group
L & L
MPC Technologies

Capabilities Required

Surface Mount Technologies
Ball Grid Array Application & Inspection with x-ray camera
Purchasing Components
Kitting
Cable Assemblies
Testing

Cost



- RF Controls Overall cost through commissioning: \$15.7M
 - includes SRF system (92 cavities), Reference system.
- Certain Control System high price components:
 - DSP: \$200 maximum x2
 - PLD: EP20K160E ~\$120 each x3
 - EP20K300E \$460 each (\$322 - 230) x1
 - EP20K600E \$1740 each (\$1218-870) x0
 - DUAL PORT MEMORY: \$70 each x8

Near-Term Schedule



- Module Design 7/1-10/1/00
 - PDR
 - Schematics “Board Design & Layout” 9/1/00 - 7/1/01
 - 1,2 PWB’s
 - FDR
 - Documentation
 - Vendor Selection 12/1/00 - 3/1/01
 - Build & Test 2-4 7/1/01 - 9/1/01
 - Build / Test 5-16 (Contract Manufacturer) 9/1/01 - 3/1/02
 - Integration

ISSUES



- FROM MEETING AT JLAB 7/13/00
 - Reference design
 - Daughterboard(s)
 - Necessary, or will it fit on single board?
 - Duroid layer required?
 - Resonance Control methodology
 - Elimination of IOC?
- OTHERS RAISED TODAY?
 - Data synchronization of FIFO's, memories, ...

Design Review Wrap-up 1



- Assumptions and Requirements: Covered above.
- Interfaces: Covered above.
- Design Criteria: Covered above.
- Engineering Analysis: Covered above.
- Reliability and Maintenance: Covered above.
- Hazard/Safety Analysis: No specific hazards are associated with the HPPS hardware. SFMEA will identify system effects due to HPPS failure.
- Cost and Schedule: Covered by Amy Regan.
- Manufacturing and QA: Covered by Irene DeBaca
- Installation and Integration: Covered by Amy Regan

Design Review Wrap-up 2



- Documentation Plan: Will provide schematics, fab drawings, parts lists, O&M manual, acceptance test instructions, and production test SW (if required).
- History and Previous Action Items: Covered above under LEDA lessons learned.