

## Evolution of the digital board

### Core functionality

The schematic and artwork for the interconnection of four 40 MS/s ADS808 ADCs, the XC2S150 FPGA, and the embedded nanoEngine computer, are kept exactly the same as before. The output channel has been reworked, and now takes the form of a direct 50 MHz output. A dedicated note describes this change in detail.

An on-board 14 dB gain preamplifier has been added to the 50 MHz ADC input channels. Second harmonic distortion is irrelevant, because it gets suppressed digitally the same way as DC offsets. The requirement for low third harmonic distortion is troublesome; the chosen solution is an OPA685, which only satisfies -60 dBc only if run from a 10 V supply.

## Connectors

The 50-pin connectors used to make the system IP-module compatible proved difficult to work with on the test bench. We never exercised the IP-module compatibility mode. The new design calls for real SMA connectors for the 50 MHz inputs and outputs, and a 100-mil header for the “auxiliary” connections on the inside of the chassis. The only host computer supported is the nanoEngine. This change also removes the PROM socket for programming the FPGA.

The 80 mil (2 mm) headers used for Ethernet, RS-232, and power proved difficult to work with on the test bench. We replace them with real RJ-45 jacks (Ethernet and RS-232), and 100-mil headers (power). This choice has a large impact on chassis construction: the board must now sit flush against a panel, to give external access to the RJ-45 connectors.

## Interlocks

The interlock interface has been updated to match the DB-9F connector of the LANL HPM design. If used in combination with the HPM, the interlocks can be effectively daisy-chained. The interlock logic is simple, and a proper subset of that formerly built on the analog board.

Pin	Function
1	MPS_PERMIT High side
2	Loop-back input from MPS
3	N/C
4	N/C
5	RF_PERMIT_HARD High side
6	MPS_PERMIT Low side
7	Loop-back output to MPS
8	N/C
9	RF_PERMIT_HARD Low side

## Phase Reference

The revised SNS phase reference system, and experience with the tangle of cables needed to make use of the previous arrangement, leads us to put the system clock on-board. Does this need to be (analog) phase locked to the 50 MHz reference? A decent PCB mount XO will have 20 ppm of drift or other inaccuracy. This translates into a 1 kHz offset at 50 MHz, so during a 1 ms pulse the phase of an acquired waveform can move around the circle once. Trying to keep track of this digitally sounds awkward at best, so I choose an analog loop instead. This assumes that the 50 MHz source provided is continuous (not pulsed) and has low phase noise. As a hedge, we will include a trimpot that can replace the PLL control of the VCXO.

## On-board Clock Distribution

Clock distribution is somewhat more complex this time, because of the choice to run the DAC at 80 MHz. The divide-by-two step needs to be done not in the FPGA, because the 40 MHz output needs to have very low jitter, and the FPGA package will be full of ground bounce.

I am amused by the statement in the ICS8737 data sheet: “The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.” My hope is that it adds less than 0.5 ps rms jitter.

Direct parallel connection of ADS808 clock lines worked well. Its skew vs. a real fanout tree is small, can be estimated ( $20 \text{ mm} / 0.8c = 0.8 \text{ ns}$ ), and ends up as part of system calibration along with all other cables. This time it is driven from an ECL gate via a transformer.

## **Low speed DAC**

Need at least one system DAC channel, to control the output RF level (402.5 MHz modulator). The DAC used previously (MAX528) needs +15V, +10V, and -5V, so we choose a new chip (MAX5742) instead. It has 12 bits resolution instead of 8, but only four channels. The three unused output channels will be made available on a connector.

## Low speed ADC

The system needs least 2 system ADC channels (VCO control and LO strength). MAX1202 known good from previous analog board.

Additional, potentially interesting channels to round out 8 on the chip:

- 5V supply voltage
- 5V supply current
- 12V supply voltage
- modulator voltage
- two spare from a connector

Input signal conditioning is not considered crucial, but we will filter them such that Nyquist sampling is possible on any one channel.  $16 \mu\text{s}$  sampling means filter needs to cut out frequencies above 30 kHz.

### **Non-essential features**

The DS2401 (serial number) and TCN75 (thermometer) are not needed to meet specifications. If they work, the system is nicer as a result. If the software breaks, they get ignored. If anything goes wrong with the hardware, they get clipped out.

At the last minute, we patched the first generation system to add four LED's for quick in-the-rack heartbeat and "input signal present" reporting. This proved extremely valuable. This time, we will put four LED's directly on-board, to assist earlier in the board commissioning process.

## **Reference Mux control**

We set aside a “spare” TTL compatible output that can mux the cavity and reference signals into a single mixer/ADC, in case that is needed. I have reservations about the amount of channel isolation that is plausible to achieve. Without that multiplexing step, a contribution to drift is the temperature and temperature coefficient mismatch between two 50 MHz analog input channels. We will have to measure that.

## Hardware checkout steps

Derived from experience with MEBT system, with new steps to cover new features.

- Power supplies regulate
- Computer boots and networks
- FPGA identifies via JTAG
- FPGA programs and flashes lights
- VCXO locks to external reference
- Four ADC channels record waveforms
- Measure ADC noise characteristics with 50 MHz input
- Send test pattern to 50 MHz output
- Check internal and external control of RF gate
- Computer reads out low speed ADC
- Computer sets low speed DAC
- Computer reads serial number and temperature

## **Firmware programming tasks**

Adapt to 80 MHz output DAC clock. Keep the existing logic running at 40 MHz for easy synthesis.

Add interlocks to kill RF if the field or reflected power behaves unexpectedly.

Update serial port handling to accommodate new devices:

- PE3239 (phase locked loop)
- MAX5742 (low speed DAC)
- TCN75 (thermometer)
- DS2401 (serial number)

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## Software enhancements

Attempt automated turn-on.

